Datasheet

APM32F107xBxC

APM32F105x8xBxC

Arm® Cortex®-M3 based 32-bit MCU

Version: V1.2

1. Product characteristics

- **Core**
  - 32-bit Arm® Cortex®-M3 core
  - Up to 96MHz working frequency
- **On-chip memory**
  - Flash：up to 256KB
  - SRAM：up to 64KB
- **Clock**
  - HSECLK: 3~25MHz external crystal/ceramic oscillator supported
  - LSECLK: 32.768KHz crystal/ceramic oscillator supported
  - HSICLK: 8MHz RC oscillator calibrated by factory
  - LSICLK: 40KHz RC oscillator supported
  - PLL: 3 configurable phase-locked loops are provided
- **Reset and power management**
  - V_{DD} range: 2.0～3.6V
  - V_{DDA} range: 2.0～3.6V
  - V_{BAT} range of backup domain power supply: 1.8V～3.6V
  - Power-on/power-down reset (POR/PDR) supported
  - Programmable power supply voltage detector supported(PVD)
- **Low-power mode**
  - Sleep, stop and standby modes supported
- **DMA**
  - Two DMA; DMA1 supports 7 channels and DMA2 supports 5 channels
- **Debugging interface**
  - JTAG
  - SWD
- **I/O**
  - Up to 80 I/Os
  - All I/Os can be mapped to external interrup vector
  - Up to 60 FT input I/Os
- **Communication peripherals**
  - 2 I2C interfaces (1Mbit/s), all of which support SMBus/PMBus
  - 3 USART, 2 UART, support ISO7816, LIN and IrDA functions
  - 3 SPI (2 reusable I2S), maximum transmission speed 18Mbps
  - 2 CAN
  - 1 USB OTG_FS Controller
  - Ethernet MAC
- **Analog peripherals**
  - 2 12-bit ADCs
  - 2 12-bit DACs
- **Timer**
  - 1 16-bit advanced timers TMR1 that can provide 7 channels PWM output, support dead zone generation and braking input functions
  - 4 16-bit general-purpose timers TMR2/3/4/5, each with up to 4 independent channels to support input capture, output comparison, PWM, pulse count and other functions
  - 2 16-bit basic timers TMR6/7
  - 2 watchdog timers: one independent watchdog IWDT and one window watchdog WWDT
  - 1 24-bit autodecrement SysTick Timer
- **RTC**
  - Support calendar functions
- **84Bytes backup register**
- **CRC computing unit**
- **96-bit unique device ID**

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2. Product information

See the following table for APM32F107 105xx product functions and peripheral configuration.

Table 1 Functions and Peripherals of APM32F107 105xx Series Chips

Product		**APM32F105**						**APM32F107**			
Model		R8T6	RBT6	RCT6	V8T6	VBT6	VCT6	RBT6	RCT6	VBT6	VCT6
Package		LQFP64			LQFP100			LQFP64		LQFP100	
Core and maximum working frequency		Arm® 32-bit Cortex®-M3@96MHz									
Operating voltage		2.0~3.6V									
Flash(KB)		64	128	256	64	128	256	128	256	128	256
SRAM(KB)		64									
GPIOs		51			80			51		80	
Communication interface	USART/UART	3/2									
	SPI/I2S	3/2									
	I2C	2						1			
	USB OTG_FS	1									
	Ethernet	0						1			
	CAN	2									
Timer	16-bit advanced	1									
	16-bit general	4									
	16-bit basic	2									
	System tick timer	1									
	Watchdog	2									
Real-time clock		1									
12-bit ADC	Unit	2									
	External channel	16									
	Internal channel	2									
12-bit DAC	Unit	2									
	Channel	2									
Operating temperature		Ambient temperature:-40°C 至 85°C Junction temperature:-40°C 至 105°C									

3. Pin information

3.1. Pin distribution

Figure 1 Distribution Diagram of APM32F107 105xx Series LQFP100 Pins

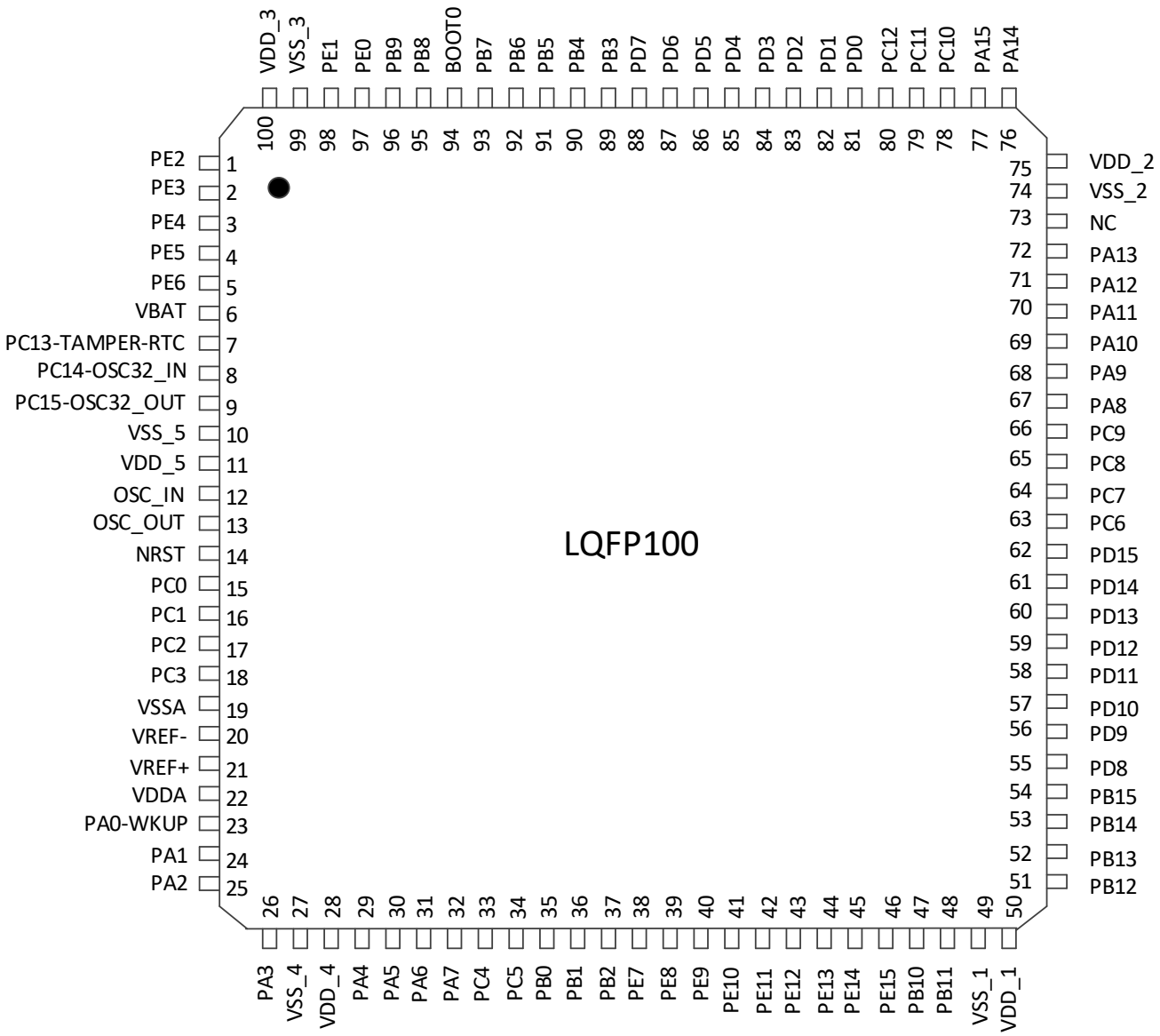
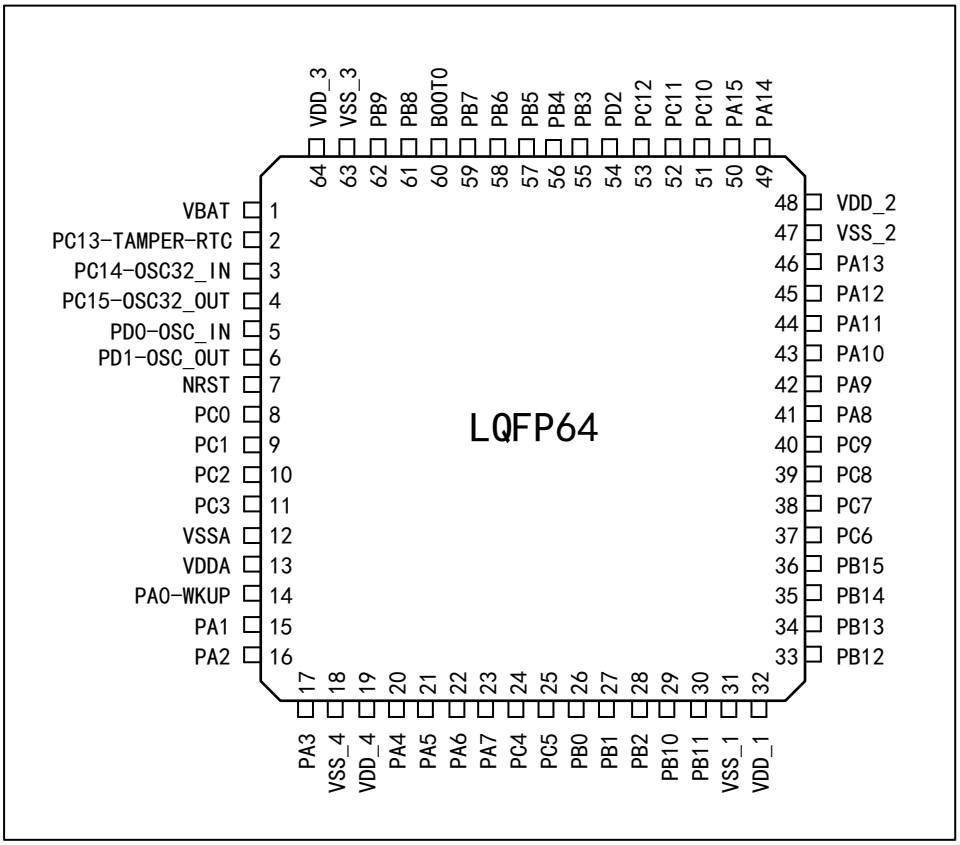


Figure 2 Distribution Diagram of APM32F107 105xx Series LQFP64 Pins



3.2. Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type	P	Power pin
	I	Only input pin
	I/O	I/O pin
I/O structure	5T	FT I/O
	5Tf	FT I/O, FM+ function
	STDA	I/O with 3.3 V standard, directly connected to ADC
	STD	I/O with 3.3 V standard
	B	Dedicated Boot0 pin
	RST	Bidirectional reset pin with built-in pull-up resistor
Note	Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	

Name		Abbreviation	Definition
Pin function	Default multiplexing function	Function directly selected/enabled through peripheral register	
	Remap	Select this function through AFIO remapping register	

Table3 Description of APM32F107 105xx by Pin Function

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP64	LQFP100
PE2	I/O	5T	TRACECK	-	-	1
PE3	I/O	5T	TRACED0	-	-	2
PE4	I/O	5T	TRACED1	-	-	3
PE5	I/O	5T	TRACED2	-	-	4
PE6	I/O	5T	TRACED3	-	-	5
V_{BAT}	P	-	-	-	1	6
PC13-TAMPER-RTC (PC13)	I/O	STD	TAMPER_RTC	-	2	7
PC14-OSC32_IN (PC14)	I/O	STD	OSC32_IN	-	3	8
PC15-OSC32_OUT (PC15)	I/O	STD	OSC32_OUT	-	4	9
V_{SS_5}	P	-	-	-	-	10
V_{DD_5}	P	-	-	-	-	11
OSC_IN	I	STD	-	-	5	12
OSC_OUT	O	STD	-	-	6	13
NRST	I/O	RST	-	-	7	14
PC0	I/O	STDA	ADC12_IN10	-	8	15
PC1	I/O	STDA	ADC12_IN11, ETH_MII_MDC, ETH_RMII_MDC	-	9	16
PC2	I/O	STDA	ADC12_IN12, ETH_MII_TXD2	-	10	17
PC3	I/O	STDA	ADC12_IN13, ETH_MII_TX_CLK	-	11	18
V_{SSA}	P	-	-	-	12	19

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP64	LQFP100
V_{REF-}	P	-	-	-	-	20
V_{REF+}	P	-	-	-	-	21
V_{DDA}	P	-	-	-	13	22
PA0-WKUP (PA0)	I/O	STDA	WKUP, USART2_CTS, ADC12_IN0, TMR2_CH1_ETR, TMR5_CH1, ETH_MII_CRS_WKUP	-	14	23
PA1	I/O	STDA	USART2_RTS, ADC12_IN1, TMR5_CH2, TMR2_CH2, ETH_MII_RX_CLK, ETH_RMII_REF_CLK	-	15	24
PA2	I/O	STDA	USART2_TX, TMR5_CH3, ADC12_IN2, TMR2_CH3, ETH_MII_MDIO, ETH_RMII_MDIO	-	16	25
PA3	I/O	STDA	USART2_RX, TMR5_CH4, ADC12_IN3, TMR2_CH4, ETH_MII_COL	-	17	26
V_{SS_4}	P	-	-	-	18	27
V_{DD_4}	P	-	-	-	19	28
PA4	I/O	STDA	SPI1_NSS, USART2_CK, DAC_OUT1, ADC12_IN4	SPI3_NSS, I2S3_WS	20	29
PA5	I/O	STDA	SPI1_SCK, DAC_OUT2, ADC12_IN5	-	21	30
PA6	I/O	STDA	SPI1_MISO, ADC12_IN6 TMR3_CH1	TMR1_BKIN	22	31
PA7	I/O	STDA	SPI1_MOSI,	TMR1_CH1N	23	32

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP64	LQFP100
			ADC12_IN7, TMR3_CH2, ETH_MII_RX_DV, ETH_RMII_CRS_DV			
PC4	I/O	STDA	ADC12_IN14 ETH_MII_RXD0, ETH_RMII_RXD0	-	24	33
PC5	I/O	STDA	ADC12_IN15, ETH_MII_RXD1, ETH_RMII_RXD1	-	25	34
PB0	I/O	STDA	ADC12_IN8, TMR3_CH3, ETH_MII_RXD2	TMR1_CH2N	26	35
PB1	I/O	STDA	ADC12_IN9, TMR3_CH4, ETH_MII_RXD3	TMR1_CH3N	27	36
PB2 (PB2,BOOT1)	I/O	5T	-	-	28	37
PE7	I/O	5T	-	TMR1_ETR	-	38
PE8	I/O	5T	-	TMR1_CH1N	-	39
PE9	I/O	5T	-	TMR1_CH1	-	40
PE10	I/O	5T	-	TMR1_CH2N	-	41
PE11	I/O	5T	-	TMR1_CH2	-	42
PE12	I/O	5T	-	TMR1_CH3N	-	43
PE13	I/O	5T	-	TMR1_CH3	-	44
PE14	I/O	5T	-	TMR1_CH4	-	45
PE15	I/O	5T	-	TMR1_BKIN	-	46
PB10	I/O	5T	I2C2_SCL, USART3_TX, ETH_MII_RX_ER	TMR2_CH3	29	47
PB11	I/O	5T	I2C2_SDA, USART3_RX, ETH_MII_TX_EN, ETH_RMII_TX_EN	TMR2_CH4	30	48
V_{SS_1}	P	-	-	-	31	49
V_{DD_1}	P	-	-	-	32	50
PB12	I/O	5T	SPI2_NSS,	-	33	51

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP64	LQFP100
			I2S2_WS, I2C2_SMBAI, USART3_CK, TMR1_BKIN, CAN2_RX, ETH_MII_TXD0, ETH_RMII_TXD0			
PB13	I/O	5T	SPI2_SCK, I2S2_CK, USART3_CTS, TMR1_CH1N, CAN2_TX, ETH_MII_TXD1, ETH_RMII_TXD1	-	34	52
PB14	I/O	5T	SPI2_MISO, TMR1_CH2N, USART3_RTS	-	35	53
PB15	I/O	5T	SPI2_MOSI, I2S2_SD, TMR1_CH3N	-	36	54
PD8	I/O	5T	-	USART3_TX, ETH_MII_RX_DV, ETH_RMII_CRS_DV	-	55
PD9	I/O	5T	-	USART3_RX, ETH_MII_RXD0, ETH_RMII_RXD0	-	56
PD10	I/O	5T	-	USART3_CK, ETH_MII_RXD1, ETH_RMII_RXD1	-	57
PD11	I/O	5T	-	USART3_CTS, ETH_MII_RXD2	-	58
PD12	I/O	5T	-	TMR4_CH1, USART3_RTS, ETH_MII_RXD3	-	59
PD13	I/O	5T	-	TMR4_CH2	-	60
PD14	I/O	5T	-	TMR4_CH3	-	61
PD15	I/O	5T	-	TMR4_CH4	-	62
PC6	I/O	5T	I2S2_MCK	TMR3_CH1	37	63
PC7	I/O	5T	I2S3_MCK	TMR3_CH2	38	64

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP64	LQFP100
PC8	I/O	5T	-	TMR3_CH3	39	65
PC9	I/O	5T	-	TMR3_CH4	40	66
PA8	I/O	5T	USART1_CK, TMR1_CH1, MCO, OTG_FS_SOF	-	41	67
PA9	I/O	5T	USART1_TX, TMR1_CH2, OTG_FS_VBUS	-	42	68
PA10	I/O	5T	USART1_RX, TMR1_CH3, OTG_FS_ID	-	43	69
PA11	I/O	5T	USART1_CTS, OTG_FS_DM, CAN1_RX, TMR1_CH4	-	44	70
PA12	I/O	5T	USART1_RTS, OTG_FS_DP, CAN1_TX, TMR1_ETR	-	45	71
PA13 (JTMS,SWDIO)	I/O	5T	-	PA13	46	72
NC	-	-	Not connected	-	-	73
V_{SS_2}	P	-	-	-	47	74
V_{DD_2}	P	-	-	-	48	75
PA14 (JTCK,SWCLK)	I/O	5T	-	PA14	49	76
PA15 (JTDI)	I/O	5T	SPI3_NSS,I2S3_WS	TMR2_CH1_ETR, PA15, SPI1_NSS	50	77
PC10	I/O	5T	UART4_TX	USART3_TX, SPI3_SCK, I2S3_CK	51	78
PC11	I/O	5T	UART4_RX	USART3_RX, SPI3_MISO	52	79
PC12	I/O	5T	UART5_TX	USART3_CK, SPI3_MOSI, I2S3_SD	53	80
PD0	I/O	5T	-	CAN1_RX,	-	81

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP64	LQFP100
(OSC_IN)				OSC_IN		
PD1 (OSC_OUT)	I/O	5T	-	CAN1_TX, OSC_OUT	-	82
PD2	I/O	5T	TMR3_ETR, UART5_RX,	-	54	83
PD3	I/O	5T	-	USART2_CTS	-	84
PD4	I/O	5T	-	USART2_RTS	-	85
PD5	I/O	5T	-	USART2_TX	-	86
PD6	I/O	5T	-	USART2_RX	-	87
PD7	I/O	5T	-	USART2_CK	-	88
PB3 (JTDO)	I/O	5T	SPI3_SCK, I2S3_CK	PB3, TRACESWO, TMR2_CH2, SPI1_SCK	55	89
PB4 (NJTRST)	I/O	5T	SPI3_MISO	PB4, TMR3_CH1, SPI1_MISO	56	90
PB5	I/O	STD	I2C1_SMBAI, SPI3_MOSI, I2S3_SD, ETH_MII_PPS_OUT, ETH_RMII_PPS_OUT	TMR3_CH2, SPI1_MOSI, CAN2_RX	57	91
PB6	I/O	5T	I2C1_SCL, TMR4_CH1	USART1_TX, CAN2_TX	58	92
PB7	I/O	5T	I2C1_SDA, TMR4_CH2	USART1_RX	59	93
BOOT0	I	B	-	-	60	94
PB8	I/O	5T	TMR4_CH3, ETH_MII_TXD3	I2C1_SCL, CAN1_RX	61	95
PB9	I/O	5T	TMR4_CH4	I2C1_SDA, CAN1_TX	62	96
PE0	I/O	5T	TMR4_ETR	-	-	97
PE1	I/O	5T	-	-	-	98
V_{SS_3}	P	-	-	-	63	99
V_{DD_3}	P	-	-	-	64	100

Note:

（1） Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively.

（2） PC13, PC14 and PC15 are supplied through the power switch since the switch only sinks a limited amount of current (3mA). The use of GPIOs from PC13 to PC15 in output mode is limited: only one GPIO can be used at a Time, the speed should not exceed 2 MHz with a maximum load of 30pF and these IOs must not be used as a current source (e.g. to drive an LED).

（3） Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BAKPR register description sections in the reference manual.

（4） This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate Function I/O and Debug Configuration section in the reference manual.

（5） SPI2/I2S2 and I2C2 are not available when the Ethernet is being used.

（6） Pin5 and pin6 in the LQFP64 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 package, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to the Alternate Function I/O and Debug Configuration section in the reference manual. The use of PD0 and PD1 in output mode is limited as they can only be used at 50 MHz in output mode.

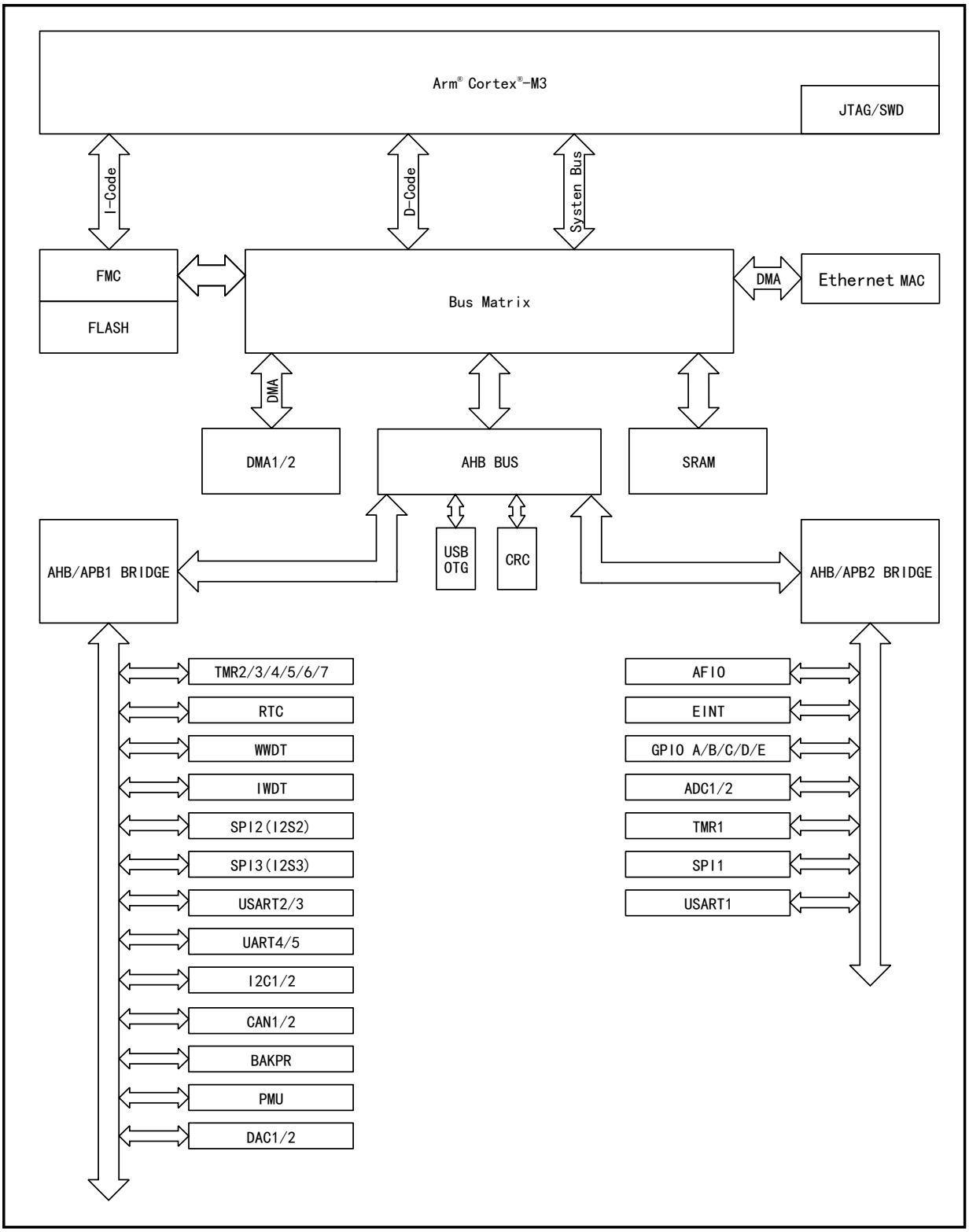
4. Functional description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32F107 105xx series products; for information about the Arm® Cortex®-M3 core, please refer to the Arm® Cortex®-M3 technical reference manual, which can be downloaded from Arm's website.

4.1. System architecture

4.1.1. System block diagram

Figure 3APM32F107 105xx System Block Diagram



4.1.2. Address mapping

Table 4 APM32F107 105xx Series Address Mapping Diagram

Region	Start Address	Peripheral Name
Code Area	0x0000 0000	Code Mapping Area
	0x0004 0000	Reserved
	0x0800 0000	Flash Main Storage Area
	0x0804 0000	Reserved
	0x1FFF B000	System Memory Area
	0x1FFF F800	Option Byte
SRAM	0x2000 0000	SRAM
—	0x2001 0000	Reserved
APB1 Bus	0x4000 0000	TMR2
	0x4000 0400	TMR3
	0x4000 0800	TMR4
	0x4000 0C00	TMR5
	0x4000 1000	TMR6
	0x4000 1400	TMR7
	0x4000 1800	Reserved
	0x4000 2800	RTC
	0x4000 2C00	WWDT
	0x4000 3000	IWDT
	0x4000 3400	Reserved
	0x4000 3800	SPI2/I2S2
	0x4000 3C00	SPI3/I2S3
	0x4000 4000	Reserved
	0x4000 4400	USART2
	0x4000 4800	USART3
	0x4000 4C00	UART4
	0x4000 5000	UART5

Region	Start Address	Peripheral Name
	0x4000 5400	I2C1
	0x4000 5800	I2C2
	0x4000 5C00	Reserved
	0x4000 6400	CAN1
	0x4000 6800	CAN2
	0x4000 6C00	BAKPR
	0x4000 7000	PMU
	0x4000 7400	DAC
	0x4000 7800	Reserved
APB2 Bus	0x4001 0000	AFIO
	0x4001 0400	EINT
	0x4001 0800	GPIOA
	0x4001 0C00	GPIOB
	0x4001 1000	GPIOC
	0x4001 1400	GPIOD
	0x4001 1800	GPIOE
	0x4001 1C00	Reserved
	0x4001 2400	ADC1
	0x4001 2800	ADC2
	0x4001 2C00	TMR1
	0x4001 3000	SPI1
	0x4001 3400	Reserved
	0x4001 3800	USART1
	0x4001 3C00	Reserved
AHB Bus	0x4002 0000	DMA1
	0x4002 0400	DMA2
	0x4002 0800	Reserved

Region	Start Address	Peripheral Name
	0x4002 1000	RCM
	0x4002 1400	Reserved
	0x4002 2000	Flash Interface
	0x4002 2400	Reserved
	0x4002 3000	CRC
	0x4002 3400	Reserved
	0x4002 8000	Ethernet
	0x4003 0000	Reserved
	0x5000 0000	USB OTG_FS
—	0x5000 0400	Reserved

4.1.3. Startup configuration

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from main memory
- Startup from BootLoader
- Startup from built-in SRAM

The user can use USART interface to reprogram the user Flash if boot from BootLoader.

4.2. Core

The core of APM32F107 105xx is Arm® Cortex®-M3. Based on this platform, the development cost is low and the power consumption is low. It can provide excellent computing performance and advanced system interrupt response, and is compatible with all Arm tools and software.

4.3. Interrupt controller

4.3.1. Nested Vector Interrupt Controller (NVIC)

It embeds a nested vectored interrupt controller (NVIC) that can handle up to 68 maskable interrupt channels (not including 16 interrupt lines of Cortex®-M3) and 16 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

4.3.2. External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 20 edge detectors, and each detector includes edge detection circuit and interrupt/event request generation circuit; each detector can be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

4.4. On-chip memory

On-chip memory includes main memory area, SRAM and information block; the information block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written into the program and cannot be erased.

Table5 On-chip Memory Area

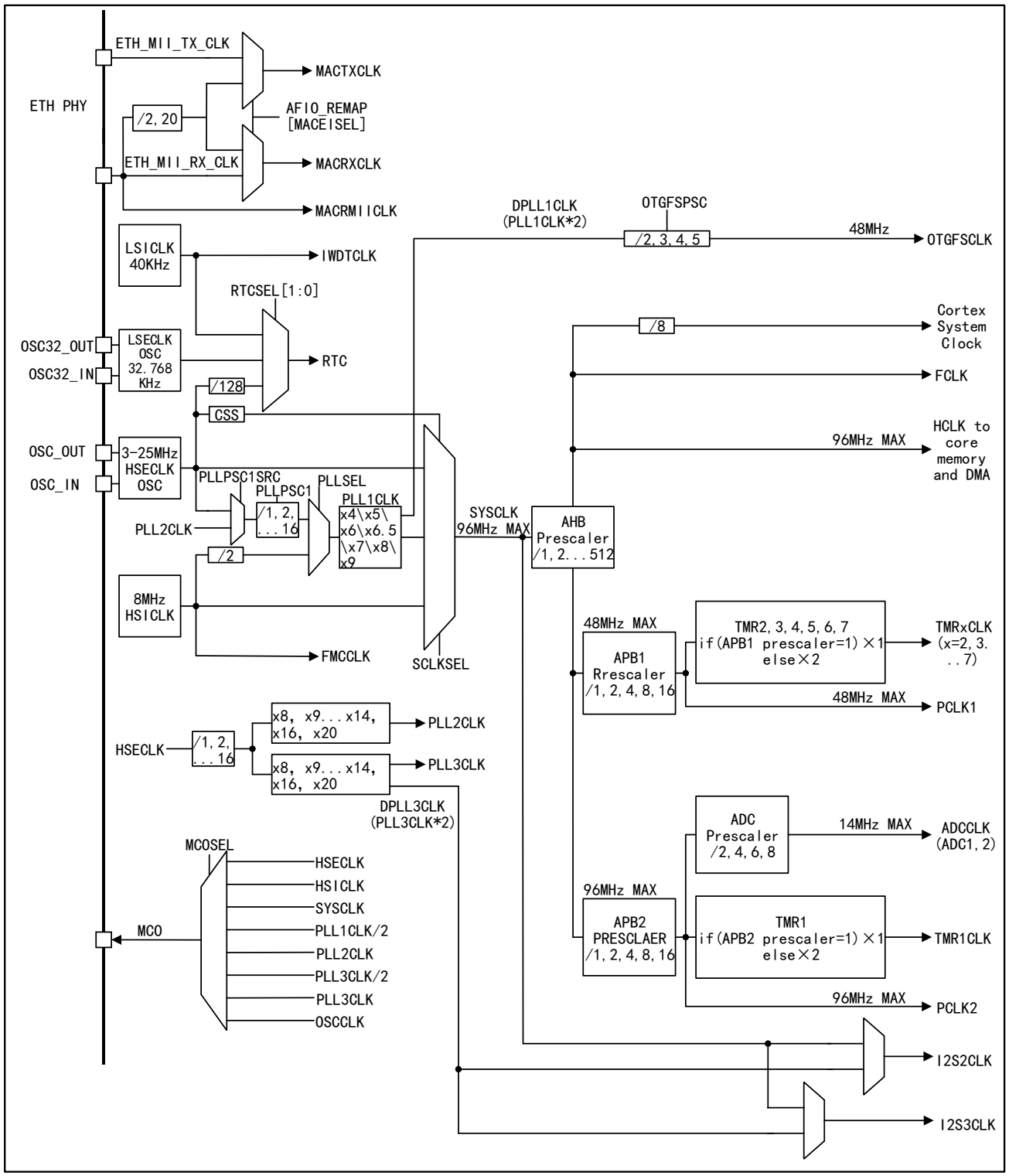
Memory	Maximum capacity	Function
Main memory area	256 KB	Store user programs and data.
SRAM	64 KB	CPU can access at 0 waiting cycle (read/write).
System memory area	18KB	Store BootLoader, 96-bit unique device ID, and main memory area capacity information
Option byte	16Bytes	Configure main memory area read-write protection and MCU working mode

4.5. Clock

4.5.1. Clock tree

Clock tree of APM32F107 105xx is shown in the figure below:

Figure 4 APM32F107 105xx Clock Tree



4.5.2. Clock source

Clock source is divided into high-speed clock and low-speed clock according to the speed; the high-speed clock includes HSICLK and HSECLK, and the low-speed clock includes LSECLK and LSICLK; clock source is divided into internal clock and external clock according to the chip inside/outside; the internal clock includes HSICLK and LSICLK, and the external clock includes HSECLK and LSECLK, among which HSICLK is calibrated by the factory to ±1% accuracy.

4.5.3. System clock

HSICLK, PLL1CLK and HSECLK can be selected as system clock; the clock source of PLL1CLK can be one of HSICLK and HSECLK; the required system clock can be obtained by configuring PLL clock multiplier factor and frequency dividing coefficient.

When the product is reset and started, HSICLK is selected as the system clock by default, and then the user can choose one of the above clock sources as the system clock by himself. When HSECLK failure is detected, the system will automatically switch to the HSICLK, and if an interrupt is enabled, the software can receive the related interrupt.

4.5.4. Bus clock

AHB, APB1 and APB2 are built in. The clock source of AHB is SYSCLK, and the clock source of APB1 and APB2 is HCLK; the required clock can be obtained by configuring the frequency dividing coefficient. The maximum frequency of AHB and high-speed APB2 is 96MHz, and the maximum frequency of APB1 is 48MHz.

4.6. Power supply and power management

4.6.1. Power supply scheme

Table6 Power Supply Scheme

Name	Voltage range	Instruction
V_{DD}	2.0～3.6V	I/Os (see pin distribution diagram for specific IO) and internal voltage regulator are powered through V_{DD} pin.
V_{DDA}/V_{SSA}	2.0～3.6V	Power supply of ADC, DAC, reset module, RC oscillator and PLL analog part; when ADC or DAC is us-ed, V_{DDA} shall not be less than 2.4V; V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.
V_{BAT}	1.8～3.6V	When V_{DD} is closed, RTC, external 32.768KHz oscillator and backup register are supplied through internal power switch.

4.6.2. Voltage regulator

Table7 Regulator Operating Mode

Name	Instruction
Master mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode, when the voltage regulator has high impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.6.3. Power supply voltage monitor

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable voltage regulator (PVD) that can monitor V_{DD} and compare it with V_{PVD} threshold. When V_{DD} is outside the V_{PVD} threshold range and the interrupt is enabled, the MCU can be set to a safe state through the interrupt service program.

4.7. Low-power mode

APM32F107 105xx supports three low-power modes, namely, sleep mode, stop mode and standby mode, and there are differences in power, wake-up time and wake-up mode among these three modes. The low-power mode can be selected according to the actual application requirements.

Table8 Low Power Consumption Mode

Mode	Instruction
Sleep mode	The core stops working, all peripherals are working, and it can be woken up through interrupts/events
Stop mode	Under the condition that SRAM and register data are not lost, the stop mode can achieve the lowest power consumption; The clock of the internal 1.5V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be prohibited, and the voltage regulator can be configured in normal mode or low power mode; Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, PVD output, RTC and USB OTG_FS.
Standby mode	The power consumption in this mode is the lowest; Internal voltage regulator is turned off, all 1.3V power supply modules are powered off, HSECLK crystal resonator, HSICLK and PLL clocks are turned off, SRAM and register data disappear, RTC area and backup register contents remain, and standby circuit still works; The external reset signal on NRST, IWDT reset, rising edge on WKUP pin or RTC event will wake MCU out of standby mode.

4.8. DMA

2 built-in DMAs; DMA1 supports 7 channels and DMA2 supports 5 channels. Each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI, USART, I2C, and TMRx. Four levels of DMA channel priority can be configured. Support "memory→memory, memory→peripheral, peripheral→memory" transfer of data (the memory includes Flash、SRAM)

4.9. GPIO

GPIO can be configured as general input, general output, multiplexing function and analog input、output. The general input can be configured as floating input, pull-up input and pull-down input; the general output can be configured as push-pull output and open-drain output; the multiplexing function can be used for digital peripherals; and the analog input and output can be used for analog peripherals and low-power mode; the enable and disable pull-up/pull-down resistor can be configured; the speed of 2MHz, 10MHz and 50MHz can be configured; the higher the speed is, the greater the power and the noise will be.

4.10. Communication peripherals

4.10.1. USART/UART

Up to 5 universal synchronous/asynchronous transmitter receivers are built in the chip. The USART1 interface can communicate at a rate of 4.5Mbit/s, while other USART/UART interfaces can communicate at a rate of 2.25Mbit/s. All USART/UART interfaces can configure baud rate, parity check bit, stop bit, and data bit length; except UART5, all the other USART/UART can support DMA. USART/UART function differences are shown in the table below:

Table9 USART/UART Function Differences

USART mode/function	USART1	USART2	USART3	UART4	UART5
Hardware flow control of modem	√	√	√	—	—
Synchronous mode	√	√	√	√	√
Smart card mode	√	√	√	—	—
IrDASIR coder-encoder functions	√	√	√	√	√
LIN mode	√	√	√	√	√
Single-line half-duplex mode	√	√	√	√	√
Support DMA function	√	√	√	√	—

Note: √ = support.

4.10.2. I2C

I2C1/2 bus interfaces are built in. I2C1/2 both can work in multiple master modes or slave modes, support 7-bit or 10-bit addressing, and support dual-slave addressing in 7-bit slave mode; the communication rate supports standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s); hardware CRC generator/checker are built in; they can operate with DMA and support SMBus 2.0 version/PMBus.

4.10.3. SPI/I2S

Three built-in SPIs, support full duplex and half duplex communication in master mode and slave mode, can use DMA controller, and can configure 4~16 bits per frame, and communicate at a rate of up to 18Mbit/s.

2 built-in I2S (multiplexed with SPI2 and SPI3 respectively), support half duplex communication in master mode and slave mode, support synchronous transmission, and can be configured with 16-bit, 24-bit and 32-bit data transfer with 16-bit or 32-bit resolution. The configurable range of audio sampling rate is 8kHz~48kHz; when one or two I2S interfaces are configured as the master mode, the master clock can be output to external DAC or decoder (CODEC) at 256 times of sampling frequency.

4.10.4. CAN

2 built-in CANs (CAN1 and CAN2 can be used at the same time), compatible with 2.0A and 2.0B (active) specification, and can communicate at a rate of up to 1Mbit/s. It can receive and send standard frame of 11-bit identifier and extended frame of 29-bit identifier. It has 3 sending mailboxes and 2 receiving FIFO, 28 3-level adjustable filters.

4.10.5. USB OTG_FS

1 USB controllers, namely, OTG_FS can support both host and slave functions to comply with the On-The-Go supplementary standard of USB 2.0 specification, and can also be configured as "Host only" or "Slave only" mode, to fully comply with USB 2.0 specification. OTG_FS clock (48MHz) is output by specific PLL1.

4.10.6. Ethernet

Provides an IEEE-802.3-2002 compatible MAC for Ethernet LAN communication over MII or RMII. This MCU requires a PHY connection to a physical LAN bus. The PHY connects to the MII port, uses 17 signals for MII or 9 signals for RMII, and can use a 25MHz clock (MII) from the kernel.

4.11. Analog peripherals

4.11.1. ADC

2 built-in ADCs with 12-bit accuracy, up to 16 external channels and 2 internal channels for each ADC. The internal channels measure the temperature sensor voltage and reference voltage respectively. A/D conversion mode of each channel has single, continuous, scan or intermittent modes, ADC conversion results can be left aligned or right aligned and stored in 16 bit data register; they support analog watchdog, and DMA.

4.11.1.1. Internal reference voltage

Built-in reference voltage V_{REFINT}, internally connected to ADC_IN17 channel, which can be obtained through ADC; V_{REFINT} provides stable voltage output for ADC.

4.11.2. DAC

Two built-in 12-bit DACs, and each corresponding to an output channel, which can be configured in 8-bit and 12-bit modes, and the DMA function is supported. The waveform generation supports noise wave and triangle wave. The conversion mode supports independent or simultaneous conversion and the trigger mode supports external signal trigger and internal timer update trigger.

4.12. Timer

1 built-in 16-bit advanced timers (TMR1), 4 general-purpose timers (TMR2/3/4/5), 2 basic timers (TMR6/7), 1 independent watchdog timer, 1 window watchdog timer and 1 system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is the peripheral of the core with automatic reloading function. When the counter is 0, it can generate a maskable system interrupt, which can be used for real-time operating system and general delay.

Table10 Function Comparison between Advanced/General-purpose/Basic and System Tick Timers

Timer type	System tick timer	Basic timer		General-purpose timer				Advanced timer
Timer name	Sys Tick Timer	TMR6	TMR7	TMR2	TMR3	TMR4	TMR5	TMR1
Counter resolution	24-bit	16 bits		16 bits				16 bits
Counter type	Down	Up		Up, down, up/down				Up, down, up/down
Prescaler coefficient	-	Any integer between 1 and 65536		Any integer between 1 and 65536				Any integer between 1 and 65536
General DMA request	-	OK		OK				OK
Capture/Comparison channel	-	-		4				4
Complementary outputs	-	No		No				Yes
Pin characteristics	-	-		There are 5 pins in total: 1-way external trigger signal input pins, 4-way channel (non-complementary channel) pins				There are 9 pins in total: 1-way external trigger signal input pins, 1-way braking input signal pins,

Timer type	System tick timer	Basic timer	General-purpose timer	Advanced timer
				3-pair complementary channel pins, 1-way channel (non-complementary channel) pins
Function Instruction	Special for real-time operating system Automatic reloading function supported When the counter is 0, it can generate a maskable system interrupt Can program the clock source	Used to generate DAC trigger signals. Can be used as a 16-bit general-purpose timebase counter.	Synchronization or event chaining function provided Timers in debug mode can be frozen. -Can be used to generate PWM output Each timer has independent DMA request generation. It can handle incremental encoder signals	It has complementary PWM output with dead band insertion When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, the timer can be frozen, and PWM output is disabled. Synchronization or event chaining function provided.

Table11 Independent Watchdog and Window Watchdog Timers

Name	Counter resolution	Counter type	Prescaler coefficient	Functional Description
Independent watchdog	12-bit	Down	Any integer between 1 and 256	The clock is provided by an internally independent RC oscillator of 40KHz, which is independent of the master clock, so it can run in stop and standby modes. The whole system can be reset in case of problems. It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. Timers in debug mode can be frozen.
Window watchdog	7-bit	Down	-	Can be set for free running. The whole system can be reset in case of problems. Driven by the master clock, it has early interrupt warning function; Timers in debug mode can be frozen.

4.13. RTC

1 RTC is built in, and there are LSECLK signal input pins (OSC32_IN and OSC32_OUT) and 1 TAMP input signal detection pin (TAMP); the clock source can select external 32.768kHz crystal oscillator, resonator or oscillator, LSICLK and HSECLK/128; it is supplied by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and RTC configuration and time data will not be lost; RTC configuration and time data are not lost in case of system resetting, software resetting and power resetting; it supports clock and calendar functions.

4.13.1. Backup register

84Bytes backup register is built in, and is supplied by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and the data in backup register will not be lost; the data in backup register will not be lost in case of system resetting, software resetting and power resetting.

4.14. CRC

A CRC (cyclic redundancy check) calculation unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

5. Electrical characteristics

5.1. Test conditions of electrical characteristics

5.1.1. Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at TA=25℃. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; on the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values.

5.1.2. Typical value

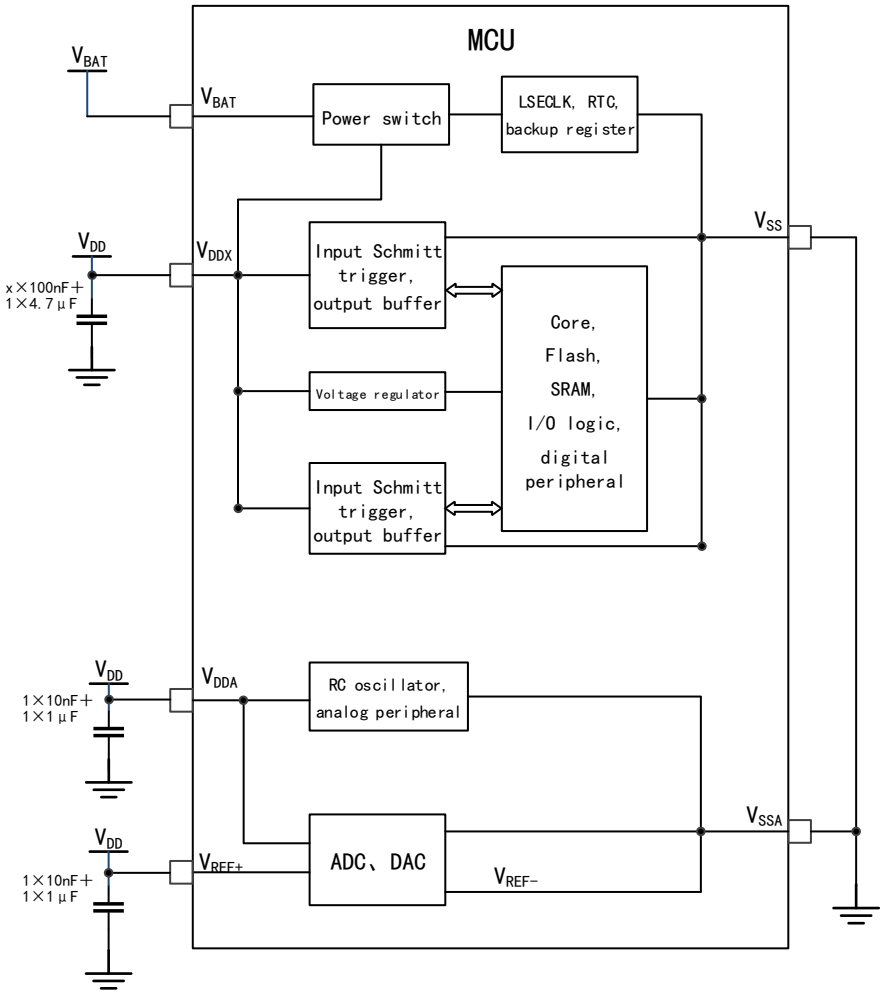
Unless otherwise specified, typical data are measured based on TA=25℃, V_{DD}=V_{DDA}=3.3V. these data are only used for design guidance.

5.1.3. Typical curve

Unless otherwise specified, typical curves will only be used for design guidance and will not be tested.

5.1.4. Power supply scheme

Figure 5 Power Supply Scheme



Notes: $V_{DD}x$ in the figure means the number of V_{DD} is x

5.1.5. Load capacitance

Figure 6 Load conditions when measuring pin parameters

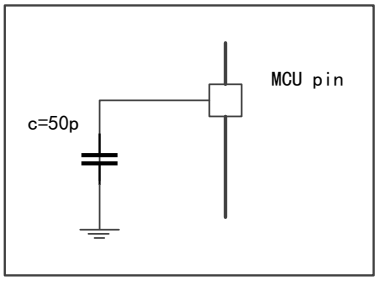


Figure 7 Pin Input Voltage Measurement Scheme

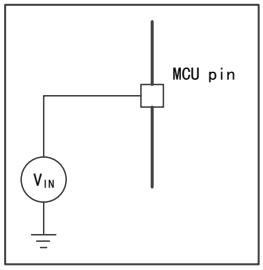
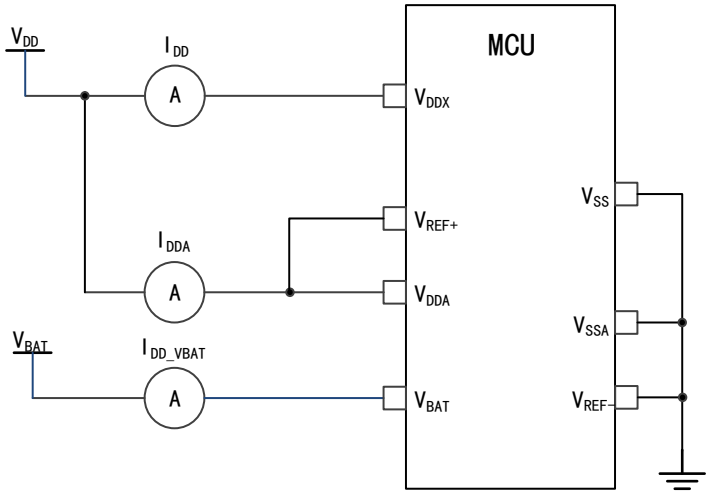


Figure 8 Power Consumption Measurement Scheme



5.2. Test under general operating conditions

Table12 General Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	96	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	48	
f_{PCLK2}	Internal APB2 clock frequency	-	-	96	
V_{DD}	Main power supply voltage	-	2	3.6	V
V_{DDA}	Analog power supply voltage (When neither ADC nor DAC is used)	Must be the same as V_{DD}	V_{DD}	3.6	V
	Analog power supply voltage (When ADC and DAC are used)		2.4	3.6	
V_{BAT}	Power supply voltage of backup domain	-	1.8	3.6	V
T_A	Ambient temperature (temperature number 6)	Maximum power dissipation	-40	85	℃

Note: During power-up and normal operation, it is recommended to use the same power supply for V_{DD} and V_{DDA}, with a maximum voltage difference of 300 mV between V_{DD} and V_{DDA}.

5.3. Absolute maximum ratings

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no

guarantee that the device functions normally under this condition.

5.3.1. Maximum temperature characteristics

Table13 Temperature Characteristics

Symbol	Description	Numerical Value	Unit
T_{STG}	Storage temperature range	-55 ~ +150	℃
T_J	Maximum junction temperature	105	℃

5.3.2. Maximum rated voltage characteristics

All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table14 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD} - V_{SS}	External main power supply voltage	-0.3	4.0	V
V_{DDA}-V_{SSA}	External analog power supply voltage	-0.3	4.0	
V_{BAT}-V_{SS}	Power supply voltage of external backup domain	-0.3	4.0	
$\lvert V_{DD}-V_{DDA} \rvert$	Voltage difference allowed by $V_{DD}>V_{DDA}$	-	0.3	
V_{IN}	Input voltage on FT pins	V_{SS}-0.3	5.5	
	Input voltage on other pins	V_{SS}-0.3	V_{DD} + 0.3	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different power supply pins	-	50	mV
$\lvert V_{SSx}-V_{SS} \rvert$	Voltage difference between different grounding pins	-	50	

5.3.3. Maximum rated current features

Table15 Current Characteristics

Symbol	Description	Maximum	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Irrigation current on any I/O and control pins	25	
	Source current on any I/O and control pins	-25	
$I_{INJ(PIN)}$ (2)	Injection current of 5T pin(3)	-5/+0	
	Injection current of other pins(4)	±5	
$\Sigma I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pins (5)	±25	

Notes:

（1） All power (V_{DD}，V_{DDA}) and ground (V_{SS}，V_{SSA}) pins must always be connected to a power supply within the external allowable range.

（2） Negative injection disturbs the analog performance of the device.

（3） Positive injection is not possible on these I/Os. a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.

（4） A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.

（5） When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.3.4. Electrostatic discharge (ESD)

Table16 ESD Absolute Maximum Ratings

Symbol	Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	TA = +25 ℃, ANSI/ESDA/JEDEC Standard, Method JS-001-2017	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	TA=+25℃, ANSI/ESDA/JEDEC Standard, Method JS-002-2018	500	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)	TA=+25℃，JEDEC Standard, Method A115-C	200	V

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.3.5. Static latch-up (LU)

Table17 Static Latch-up

Symbol	Parameter	Conditions	Type
LU	Class of static latch-up	T_A = +105℃，EIA/JEDEC STANDARD 78E	Ⅱlevel A

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.4. On-chip memory

5.4.1. Flash characteristics

Table18 Flash Memory Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
t_{prog}	16-bit programming time	T_A = -40~105℃ V_{DD}=2.4~3.6V	40	70	75	μs
t_{ERASE}	Page (2KBytes) erase time	T_A = -40~105℃ V_{DD}=2.4~3.6V	5	7	10	ms
t_{ME}	Whole erase time	T_A = 40~105℃ V_{DD}=3.3V	6	8.9	10	ms
V_{prog}	Programming voltage	T_A = -40~105℃	2	-	3.6	V
t_{RET}	Data saving time	T_A=125℃	10.77	-	-	years
N_{RW}	Erase cycle	T_A=85°C	100K	-	-	cycles

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5. Clock

5.5.1. Characteristics of external clock source

5.5.1.1. High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table19 HSECLK3~25MHz Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	25	MHz
R_F	Feedback resistance	-	-	200	-	kΩ
$I_{DD(HSECLK)}$	HSECLK current consumption	V_{DD}=3.3V, CL=10pF@8MHz	-	-	1	mA
I	HSECLK drive current	V_{DD}=3.3 V， V_{IN} =V_{SS}	-	-	1.15	mA
$t_{SU(HSECLK)}$	Startup time	V_{DD} is stable	-	2	-	ms

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.1.2. Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table20 LSECLK Oscillator Characteristics (f_{LSECLK}=32.768KHz)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{OSF_IN}	Oscillator frequency	-	-	32.768	-	KHz
$I_{DD(LSECLK)}$	LSECLK current consumption	-	-	-	1	μA
I	LSECLK drive current	V_{DD}=3.3 V， V_{IN} =V_{SS}	-	-	1.4	uA
$t_{SU(LSECLK)}$(1)	Startup time	V_{DDIOx} is stable	-	2	-	s

Note: It is obtained from a comprehensive evaluation and is not tested in production.

（1） $t_{SU(LSECLK)}$ is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

5.5.2. Characteristics of internal clock source

5.5.2.1. High speed internal (HSICLK) RC oscillator

Table21 HSICLK Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{HSICLK}	Frequency	-	-	8	-	MHz

Symbol	Parameter	Conditions		Minimum value	Typical value	Maximum value	Unit
$A_{CCHSICLK}$	Accuracy of HSICLK oscillator	Factory calibration	V_{DD}=3.3V，T_A=25℃(1)	-1	-	1	%
			V_{DD}=3.3V，T_A=-40~105℃	-2	-	2.5	%
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	-		-	-	100	μA
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD}=3.3V，T_A=-40~105℃		1	-	2	μs

Note: Except for (1) calibration in production, other data are obtained in comprehensive evaluation instead of in production.

5.5.2.2. Low speed internal (LSICLK) RC oscillator

Table22 LSICLK Oscillator Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{LSICLK}	Frequency (V_{DD} =2-3.6V, T_A =-40~105℃)	30	54	70	KHz
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator	-	1	1.1	μA
$t_{SU(LSICLK)}$	LSICLK oscillator startup time, (V_{DD}=3.3V, T_A=-40~105℃)	-	-	80	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.3. PLL Characteristics

Table23 PLL1 Characteristics

Symbol	Parameter	Minimum value	Maximum value	Unit
f_{PLL1_IN}	PLL1 input clock	3	12	MHz
	PLL1 input clock duty cycle	40	60	%
f_{PLL1_OUT}	PLL1 frequency doubling output clock, (V_{DD}=3.3V, T_A=-40~105℃)	18	96	MHz
$f_{DPLL1CLK}$	Frequency of DPLL1CLK	36	144	MHz
t_{LOCK1}	PLL1 phase locking time	-	350	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table24 PLL2 Characteristics

Symbol	Parameter	Minimum value	Maximum value	Unit
f_{PLL2_IN}	PLL2 input clock	3	5	MHz
	PLL2 input clock duty cycle	40	60	%
f_{PLL2_OUT}	PLL2 frequency doubling output clock, (V_{DD}=3.3V, T_A=-40~105℃)	18	96	MHz
$f_{DPLL2CLK}$	Frequency of DPLL2CLK	80	148	MHz
t_{LOCK2}	PLL2 phase locking time	-	350	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table25 PLL3 Characteristics

Symbol	Parameter	Minimum value	Maximum value	Unit
f_{PLL3_IN}	PLL3 input clock	3	5	MHz
	PLL3 input clock duty cycle	40	60	%
f_{PLL3_OUT}	PLL3 frequency doubling output clock, (V_{DD}=3.3V, T_A=-40~105℃)	18	96	MHz
$f_{DPLL3CLK}$	Frequency of DPLL3CLK	80	148	MHz
t_{LOCK3}	PLL3 phase locking time	-	350	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.6. Reset and power management

5.6.1. Power-on/power-down characteristics

Table26 Power-on/power-down Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{VDD}	V_{DD} rise time rate	-	7	-	200000	μs/V
	V_{DD} fall time rate		5	-	200000	

5.6.2. Test of embedded reset and power control block characteristics

Table27 Embedded Reset and Power Control Block Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.84	1.88	1.96	V
		Rising edge	1.84	1.92	2.00	V
$V_{PDRhyst}$	PDR hysteresis	-	-	54	-	mV
$T_{RSTTEMPO}$	Reset duration	-	1	2.5	4.5	ms

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table28 Programmable Power Supply Voltage Detector Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Programmable power supply voltage detector voltage level selection	PLS[2:0]=000 (rising edge)	2.15	2.17	2.18	V
		PLS[2:0]=000 (falling edge)	2.05	2.07	2.08	V
		PLS[2:0]=000(PVD hysteresis)	100.00	102.75	110.00	mV
		PLS[2:0]=001 (rising edgeg)	2.25	2.27	2.28	V
		PLS[2:0]=001 (falling edge)	2.14	2.16	2.17	V
		PLS[2:0]=001(PVD hysteresis)	110.00	110.75	120.00	mV

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
		PLS[2:0]=010 (rising edgeg)	2.35	2.37	2.38	V
		PLS[2:0]=010 (falling edge)	2.24	2.26	2.27	V
		PLS[2:0]=010(PVD hysteresis)	100.00	108.50	110.00	mV
		PLS[2:0]=011 (rising edgeg)	2.44	2.46	2.48	V
		PLS[2:0]=011 (falling edge)	2.34	2.36	2.37	V
		PLS[2:0]=011(PVD hysteresis)	100.00	103.75	110.00	mV
		PLS[2:0]=100 (rising edgeg)	2.54	2.57	2.58	V
		PLS[2:0]=100 (falling edge)	2.43	2.45	2.47	V
		PLS[2:0]=100(PVD hysteresis)	110.00	111.00	120.00	mV
		PLS[2:0]=101 (rising edgeg)	2.64	2.66	2.68	V
		PLS[2:0]=101 (falling edge)	2.53	2.56	2.57	V
		PLS[2:0]=101(PVD hysteresis)	100.00	104.50	110.00	mV
		PLS[2:0]=110 (rising edgeg)	2.74	2.76	2.78	V
		PLS[2:0]=110 (falling edge)	2.63	2.65	2.67	V
		PLS[2:0]=110(PVD hysteresis)	110.00	111.75	120.00	mV
		PLS[2:0]=111 (rising edgeg)	2.84	2.87	2.89	V
		PLS[2:0]=111 (falling edge)	2.73	2.76	2.77	V
		PLS[2:0]=111(PVD hysteresis)	110.00	116.75	120.00	mV

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.7. Power consumption

5.7.1. Power consumption test environment

（1） The values are measured by executing Dhrystone 2.1, with the Keil.V5 compilation environment and the L0 compilation optimization level.

（2） All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)

（3） Unless otherwise specified, all peripherals are turned off

（4） The relationship between Flash waiting cycle setting and f_{HCLK} :

0~24MHz: 0 waiting cycle

24~48MHz: 1 waiting cycle

48~72MHz: 2 waiting cycles

72~96MHz: 3 waiting cycles

（5） The instruction prefetch function is enabled (Note: it must be set before clock setting and bus frequency division)

（6） When the peripherals are enabled: $f_{PCLK1}=f_{HCLK}/2$，$f_{PCLK2}=f_{HCLK}$

5.7.2. Power consumption in run mode

Table29 Power Consumption in Run Mode when the Program is Executed in Flash or SRAM

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in run mode	HSECLK bypass (2) , enabling all peripherals	96MHz	292.54	34.10	329.73	36.52
		72MHz	231.43	24.35	261.72	27.11
		48MHz	183.29	15.87	208.27	17.83
		36MHz	168.03	12.93	191.62	14.67
		24MHz	148.38	8.59	170.88	9.94
		16MHz	161.26	6.11	184.31	7.09
		8MHz	17.84	3.43	24.60	4.24
	HSECLK bypass (2) , turning off all peripherals	96MHz	292.11	28.64	329.06	30.76
		72MHz	231.12	20.21	261.44	22.84
		48MHz	183.10	12.97	208.07	15.12
		36MHz	167.95	10.61	191.50	12.45
		24MHz	148.31	7.16	170.67	8.39
		16MHz	161.23	5.09	184.15	6.10
		8MHz	17.83	2.92	24.59	3.76
	HSICLK (2) , enabling all peripherals	36MHz	183.67	14.62	196.07	15.69
		24MHz	161.20	10.09	172.59	11.36
		16MHz	175.80	7.14	188.42	8.04
		8MHz	114.04	4.04	124.36	4.67
	HSICLK (2) , turning off all peripherals	36MHz	183.52	12.11	196.40	13.36
		24MHz	161.15	8.44	172.67	9.55
		16MHz	175.79	6.00	188.49	6.83
		8MHz	114.03	3.47	124.25	4.53

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

5.7.3. Power consumption in sleep mode

Table30 Power Consumption in Sleep Mode when the Program is Executed in Flash or SRAM

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=105℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA）	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in sleep mode	HSECLK bypass (2) , enabling all peripherals	96 MHz	376.86	12.27	423.00	13.06
		72MHz	242.56	9.36	274.46	9.58
		48MHz	194.82	6.61	221.60	7.18
		36MHz	179.99	5.68	204.54	6.13
		24MHz	157.53	4.08	181.12	4.65
		16MHz	172.24	3.05	196.76	3.56
		8MHz	111.03	1.94	132.61	2.44
	HSECLK bypass (2) , turning off all peripherals	96 MHz	376.19	4.66	423.80	5.14
		72MHz	242.28	3.61	274.45	4.00
		48MHz	194.68	2.74	221.70	3.22
		36MHz	179.90	2.44	205.52	2.90
		24MHz	157.45	1.94	181.58	2.41
		16MHz	172.15	1.63	197.04	2.11
		8MHz	111.02	1.22	133.28	1.73
	HSICLK (2) , enabling all peripherals	36MHz	183.47	5.71	196.38	6.56
		24MHz	160.89	4.08	172.68	4.53
		16MHz	175.62	3.06	188.03	3.53
		8MHz	113.95	1.94	123.99	2.39
	HSICLK (2) , turning off all peripherals	36MHz	183.41	2.44	196.20	2.87
		24MHz	160.80	1.93	172.43	2.37
		16MHz	175.55	1.63	187.81	2.07
		8MHz	113.94	1.22	123.89	1.66

Note:

(1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL

5.7.4. Power consumption in stop mode and standby mode

Table31 Power Consumption in Stop Mode and Standby Mode

Parameter	Conditions	Typical value (1), (T_A=25℃)						Maximum value (1), (V_{DD}=3.6V)		Unit
		V_{DD}=2.4V		V_{DD}=3.3V		V_{DD}=3.6V		T_A=105℃		
		I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	I_{DD}	
Power consumption in stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	3.667	42.441	4.282	42.169	4.594	43.11	6.16	386.35	μA
	Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	3.662	32.30	4.282	32.093	4.589	32.623	6.18	353.42	
Power consumption in standby mode	Low-speed internal RC oscillator and independent watchdog ON	2.885	0.164	3.781	0.346	4.218	0.503	5.32	4.74	
	Low-speed internal RC oscillator on, independent watchdog OFF	2.883	0.042	3.781	0.189	4.221	0.323	5.30	4.41	
	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	2.336	0.01	2.957	0.064	3.271	0.018	4.43	3.95	

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.7.5. Backup domain power consumption

Table32 Backup Domain Power Consumption

Symbol	Conditions	Typical value (1), T_A=25℃			Maximum value (1), V_{BAT}=3.6V			Unit
		V_{BAT}=2.0V	V_{BAT}=2.4V	V_{BAT}=3.3V	T_A=25℃	T_A=85℃	T_A=105℃	
$I_{DD}\_V_{BAT}$	The low-speed oscillator and RTC are in ON state	0.867	0.956	1.278	1.5	2.4	3.5	μA

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.7.6. Peripheral power consumption

The HSECLK Bypass 1M is adopted as clock source, f_{PCLK}=f_{HCLK}=1M.

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table33 Peripheral Power Consumption

Parameter	Peripheral	Typical value (1) T_A =25℃, V_{DD} =3.3V	Unit
AHB	DMA1	0.09	mA
	DMA2	0.07	
	CRC	0.71	
	Ethernet	1.08	
	USB OTG_FS	1.75	
APB1	TMR2	0.29	
	TMR3	0.26	
	TMR4	0.26	
	TMR5	0.26	
	TMR6	0.05	
	TMR7	0.05	
	WWDT	0.80	
	IWDT	0.06	
	SPI2/I2S2	0.24	
	SPI3/I2S3	0.05	
	USART2	0.10	
	USART3	0.09	
	UART4	0.09	
	UART5	0.10	
	I2C1	0.07	
	I2C2	0.08	
	CAN1	0.15	
	CAN2	0.14	
	BAKPR	0.01	
	DAC	0.05	
	PMU	0.03	
APB2	GPIOA	0.08	
	GPIOB	0.11	
	GPIOC	0.10	
	GPIOD	0.10	
	GPIOE	0.10	
	ADC1	0.33	

Parameter	Peripheral	Typical value (1) T_A =25℃, V_{DD} =3.3V	Unit
	ADC2	0.31	
	TMR1	0.38	
	SPI1	0.19	
	USART1	0.17	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.8. Wake-up time in low power mode

The measurement of wake-up time in low power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table34 Wake Up Time in Low-power Mode

Symbol	Parameter	Conditions	Min	Typical value (T_A=25℃)			Max	Unit
				2V	3.3V	3.6V		
$t_{WUSLEEP}$	Wake-up from sleep mode	-	0.51	0.58	0.57	0.58	0.64	μs
t_{WUSTOP}	Wake up from stop mode	The voltage regulator is in run mode	1.78	2.18	1.88	1.83	2.22	
		The voltage regulator is in low power mode	2.58	4.06	2.90	2.77	4.55	
$t_{WUSTDBY}$	Wake up from standby mode	-	62.78	80.03	68.63	66.97	93.10	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.9. Pin characteristics

5.9.1. I/O pin characteristics

Table35 DC Characteristics (test condition of V_{DD}=2.7~3.6V, T_A=-40~105℃)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{IL}	Standard I/O low level input voltage	-	-0.3	-	0.28*(V_{DD}-2V)+0.8V	V
	I/O FT low level input voltage	-	-0.3	-	0.32*(V_{DD}-2V)+0.75V	
V_{IH}	Standard I/O high level input voltage	-	0.41*(VDD-2V)+1.3V	-	VDD+0.3	
	I/O FT high level input voltage	V_{DD}>2V	0.42*(VDD-2V)+1V	-	5.5	
		V_{DD}≤2V			5.2	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis	-	200	-	-	mV
	I/O FT Schmitt trigger voltage hysteresis		5%V_{DD}	-	-	mV

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
I_{lkg}	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/O port	-	-	±1	μA
		V_{IN}=5V, I/O FT port	-	-	3	
R_{PU}	Weak pull-up equivalent resistance of all pins except PA10	$V_{IN}=V_{SS}$	30	40	50	kΩ
	Weak pull-up equivalent resistance of PA10		8	11	15	
R_{PD}	Weak pull-down equivalent resistance of all pins except PA10	$V_{IN}=V_{DD}$	30	40	50	
	Weak pull-down equivalent resistance of PA10		8	11	15	
C_{IO}	IO pin capacitance	-	-	2.6	-	pF

Note: It is obtained from a comprehensive evaluation and is not tested in production.

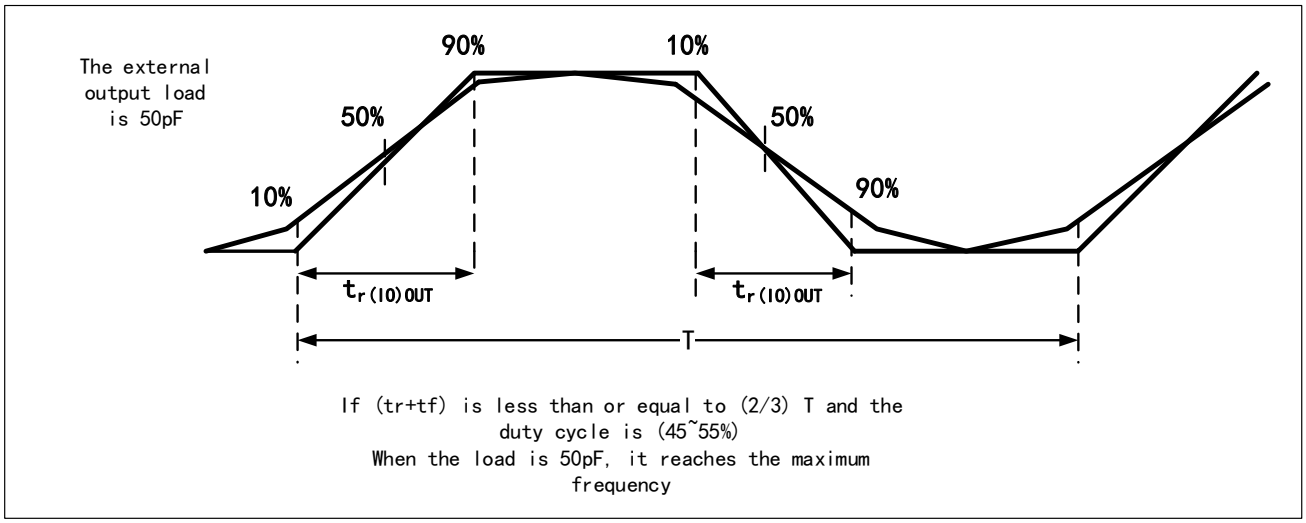
Table36 AC Characteristics

MODEy[1:0] Configuration	Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
10 (2MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50 pF, V_{DD}=2~3.6V	-	2	MHz
	$t_{f(IO)out}$	Output fall time from high to low level	C_L=50 pF, V_{DD} =2~3.6V	-	125	ns
	$t_{r(IO)out}$	Output rise time from low to high level		-	125	
01 (10MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50 pF, V_{DD} =2~3.6V	-	10	MHz
	$t_{f(IO)out}$	Output fall time from high to low level	C_L=50 pF, V_{DD} =2~3.6V	-	25	ns
	$t_{r(IO)out}$	Output rise time from low to high level		-	25	
11 (50MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50 pF, V_{DD} =2.7~3.6V	-	50	MHz
	$t_{f(IO)out}$	Output fall time from high to low level	C_L=50 pF, V_{DD} =2.7~3.6V	-	12	ns
	$t_{r(IO)out}$	Output rise time from low to high level		-	12	

Note: (1) The rate of I/O port can be configured through the corresponding register (see the user manual).

(2) The data are obtained from a comprehensive evaluation and is not tested in production.

Figure 9 I/O AC Characteristics Definition



Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table37 Output Drive Current Characteristics (test condition V_{DD}=2.7~3.6V, T_A=-40~105℃)

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
V_{OL}	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +8mA 2.7V<V_{DD}<3.6V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}-0.4	-	
V_{OL}	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20mA 2.7V<V_{DD}<3.6V	-	1.3	V
V_{OH}	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}-1.3	-	

5.9.2. NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}.

Table38 NRST Pin Characteristics (test condition V_{DD}=3.3V, T_A=-40~105℃)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{IL(NRST)}$	NRST low level input voltage	-	-0.5	-	2	V
$V_{IH(NRST)}$	NRST high level input voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
RPU	Weak pull-up equivalent resistance	V_{IN} = V_{SS}	30	40	50	kΩ

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.10. Communication peripherals

5.10.1. I2C peripheral characteristics

To achieve maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz. To

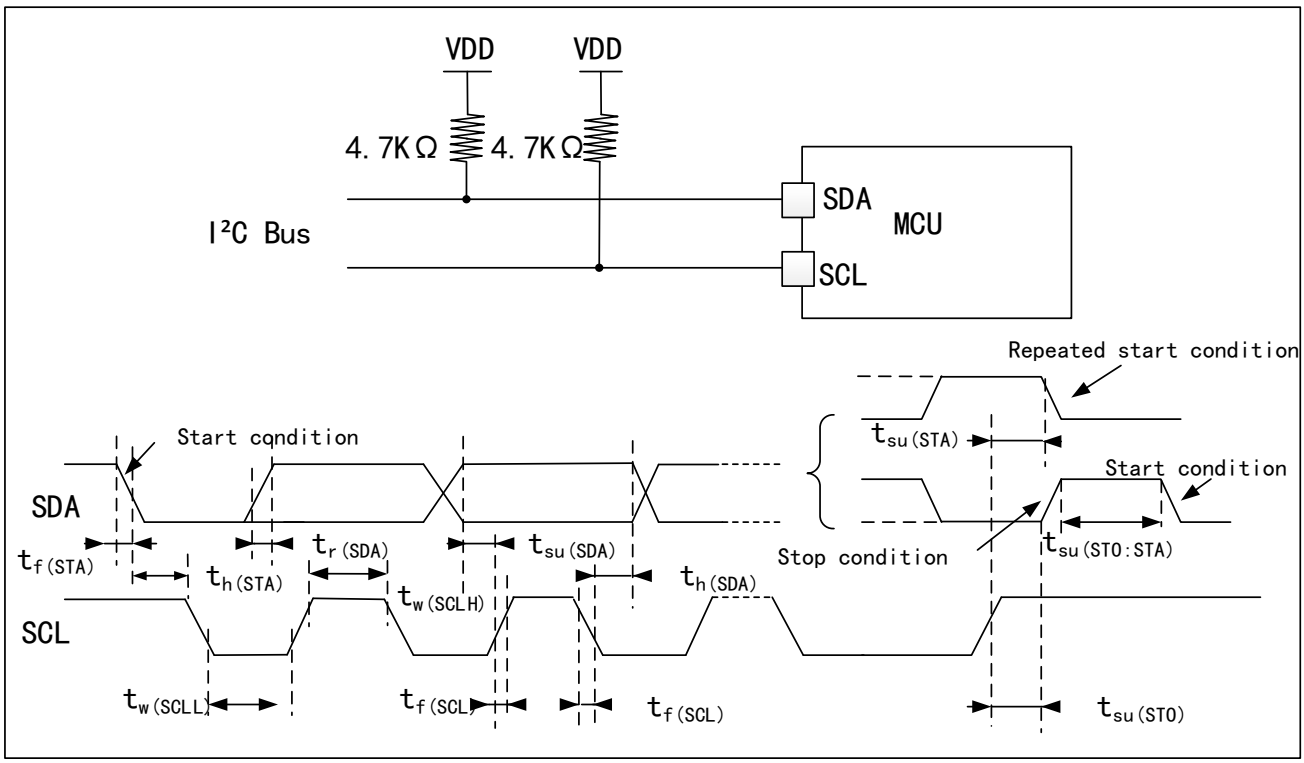
achieve maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.

Table39 I2C Interface Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900	
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	500	
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Repeated start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Setup time of stop condition	4.0	-	0.6	-	
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 10 I2C Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.10.2. SPI peripheral characteristics

Table40 SPI Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SI clock rise and fall time	Load capacitance: C = 30pF	-	8	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Main mode, f_{PCLK} = 36MHz, Prescaler coefficient=4	50	60	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	ns
		Slave mode	5	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	5	-	ns
		Slave mode	5	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20MHz	-	$3t_{PCLK}$	ns
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)	-	34	ns
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)	-	8	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	11.5	-	ns
$t_{h(MO)}$		Master mode (after enable edge)	1	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 11 SPI Timing Diagram - Slave Mode and CPHA=0

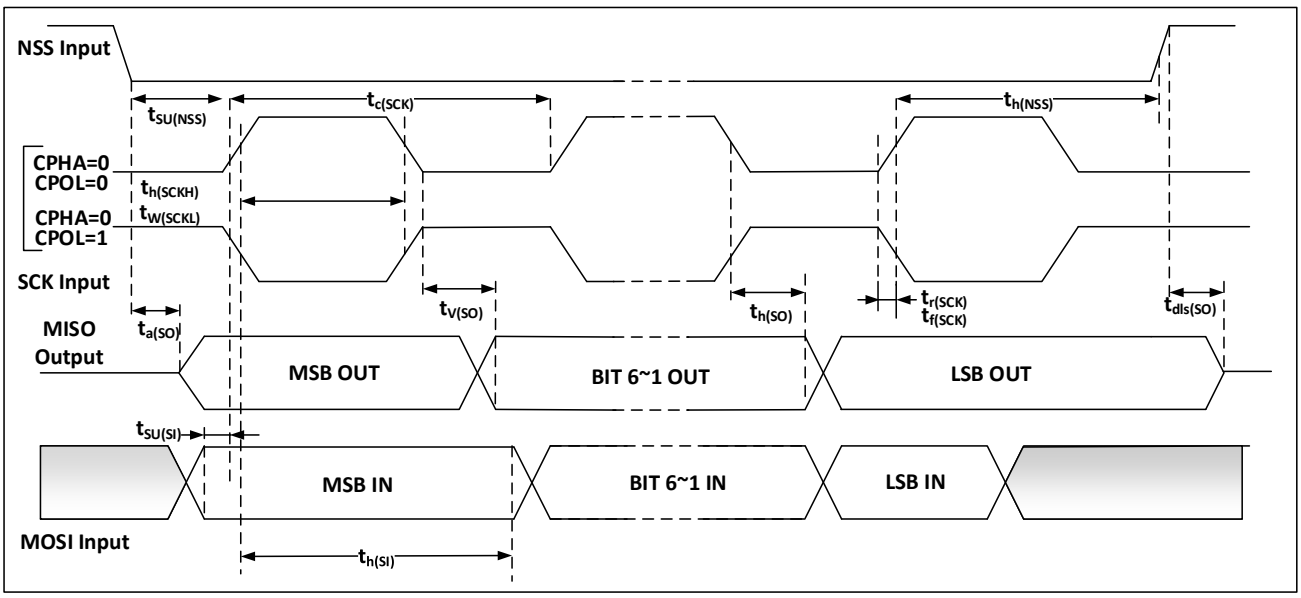
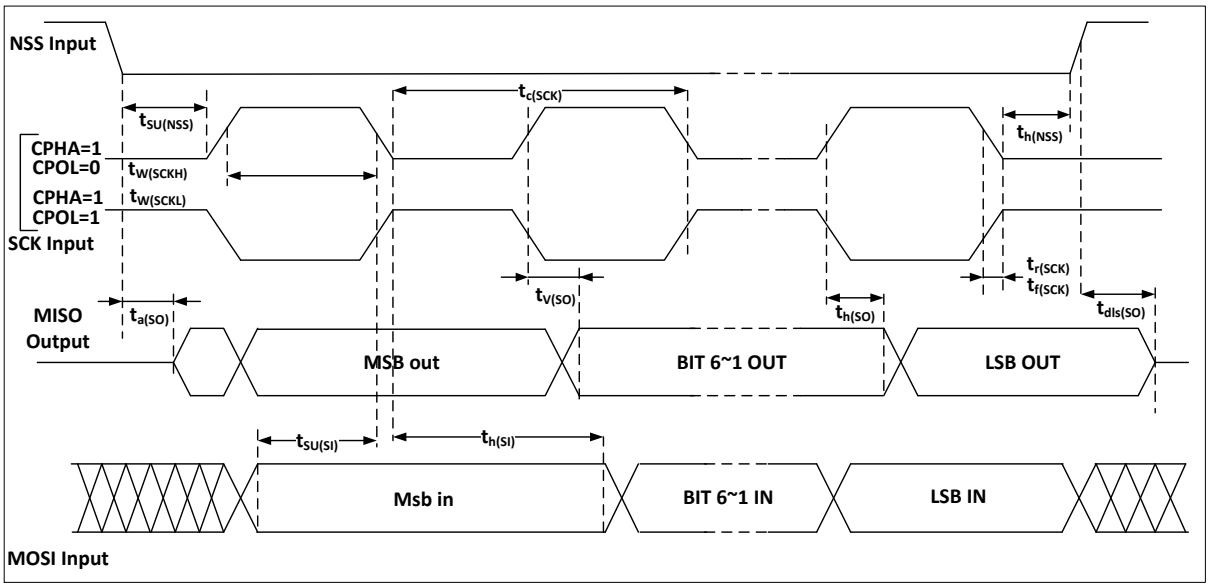
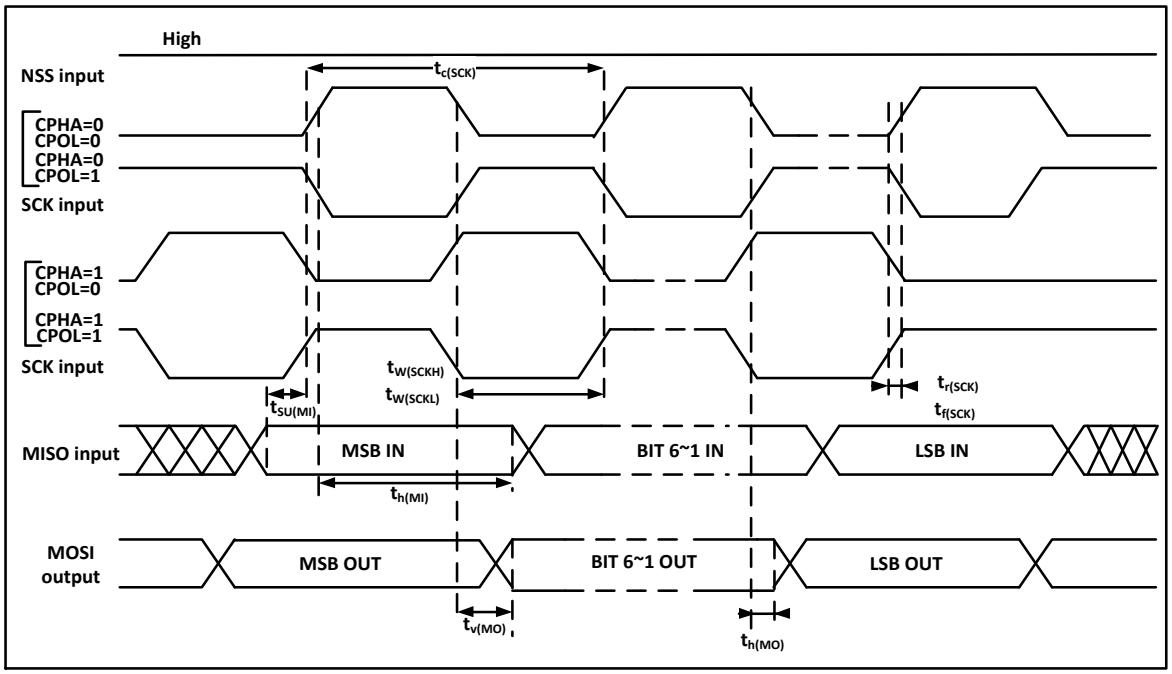


Figure 12 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 13 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.11. Analog peripherals

5.11.1. ADC

Test parameter description:

- Sampling rate: the number of conversion of analog quantity to digital quantity by ADC per second

Sample rate=ADC clock/(number of sampling periods + number of conversion periods)

5.11.1.1. 12-bit ADC characteristics

Table41 12-bit ADC Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Power supply voltage	-	2.4	-	3.6	V
f_{ADC}	ADC frequency	-	0.6	-	14	MHz
C_{ADC}	Internal sample and hold capacitor	-	-	-	2.63	pF
R_{ADC}	Sampling switch resistance	-	-	-	121	Ω
C_{ADC}	Internal sampling and holding capacitance	-	-	-	8	pF
R_{ADC}	Sampling resistor	-	-	-	1000	Ω
t_S	Sampline Time	f_{ADC}=14MHz	0.107	-	17.1	μs
T_{CONV}	Sampling and conversion time	f_{ADC}=14MHz, 12-bit conversion	1	-	18	μs

Table42 12-bit ADC Accuracy

Symbol	Parameter	Condition	Typical value	Maximum value	Unit
E_T	Total uncorrected error	f_{PCLK}=56MHz, f_{ADC}=14MHz, V_{DDA}=2.4V-3.6V T_A=-40℃~105℃	±2	±5	LSB
E_O	offset error		±1.5	±2.5	
E_G	Gain error		±1.5	±3	
E_D	Differential linear error		±1	±2	
E_L	Integral linearity error		±1.5	±3	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.1.2. Test of Built-in Reference Voltage Characteristics

Table43 Embedded Reference Voltage Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{REFINT}	Built-in Reference Voltage	-40℃ < TA < +105℃ V_{DD}= 2-3.6 V	1.16	1.20	1.26	V
$T_{S\_vrefint}$	Sampling time of ADC when reading out internal reference voltage	-	-	5.1	17.1	μs
T_{coeff}	Temperature coefficient	-	-	-	100	ppm/℃

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.2. DAC

Test parameter description:

- DNL differential non-linear error: the deviation between two consecutive codes is-1 LSB
- INL integral non-linear error: the difference between the measured value at code i and the value at code i on the connection between code 0 and the last code 4095

Table44 DAC Characteristics

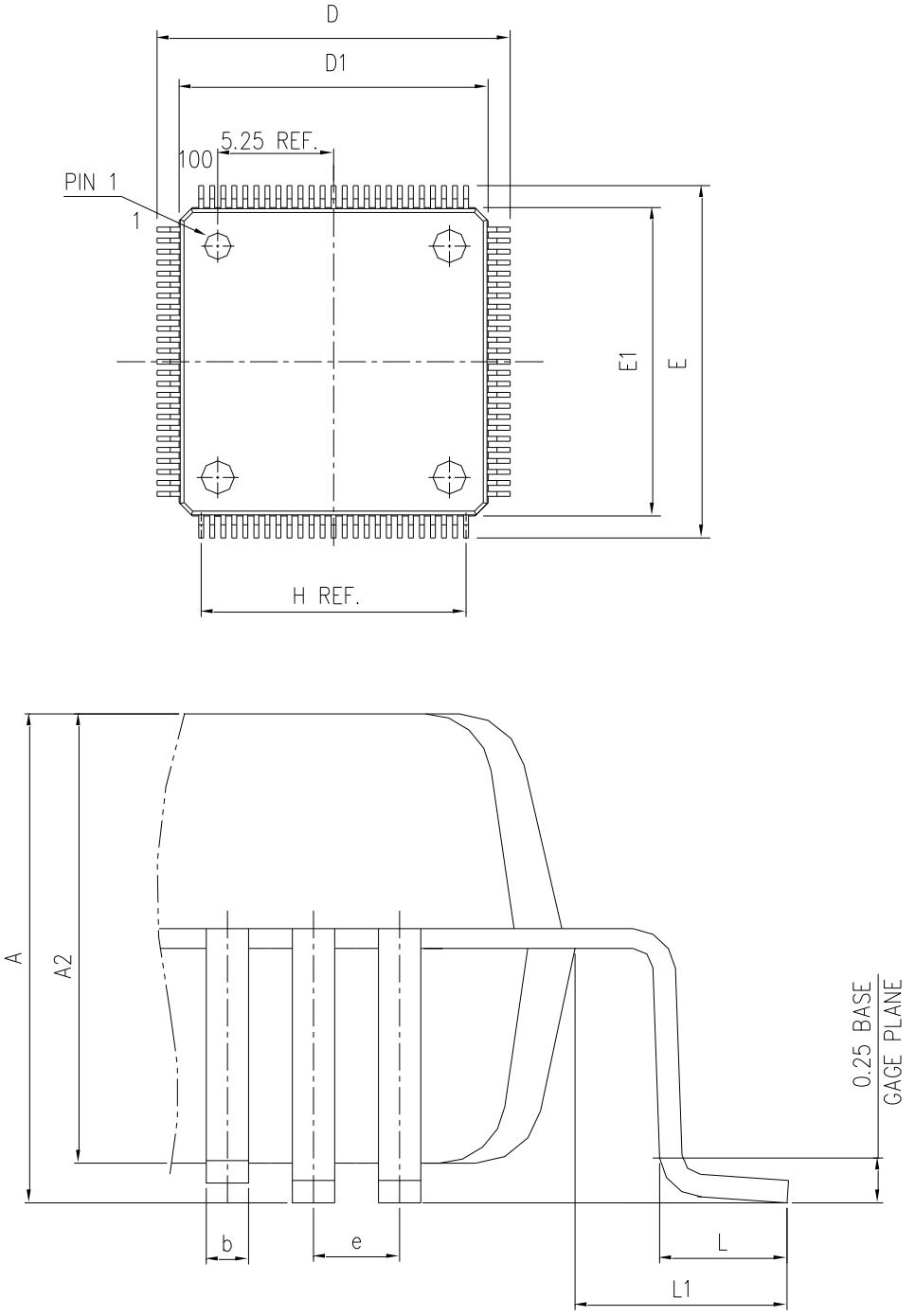
Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Analog power supply voltage	-	2.4	-	3.6	V
R_{LOAD}	Resistive load	Load is connected to VSSA with buffer on	5	-	-	kΩ
R_O	Output impedance	The resistive load between DAC_OUT and VSS is 1.5MΩ with buffer off	-	-	15	kΩ
C_{LOAD}	Capacitive load	Maximum capacitive load at DAC_OUT pin with buffer on	-	-	50	pF
DAC_OUT min	Low DAC_OUT voltage with buffer	Maximum output offset of DAC, (0x0E1) corresponding to 12-bit input code to V_{REF+}= (0xF1B) at 3.6V and V_{REF+}= (0x154) at 2.4V and (0xEAC)	0.2	-	-	V
DAC_OUT max	High output voltage with buffer		-	-	V_{DDA} – 0.2	V
DNL	Differential non-linear error	Configured with 12-bit DAC	-	-	±2.5	LSB
INL	Integral non-linear error	Configured with 12-bit DAC	-	-	±4	LSB
Offset	Offset error	V_{REF+}=3.6V, configuring 12-bit DAC	-	-	±12	LSB
Gain error	Gain error	Configured with 12-bit DAC	-	-	±0.5	%

Note: It is obtained from a comprehensive evaluation and is not tested in production.

6. Package information

6.1. LQFP100 package diagram

Figure 14 LQFP100 Package Diagram



（1） The figure is not drawn to scale.

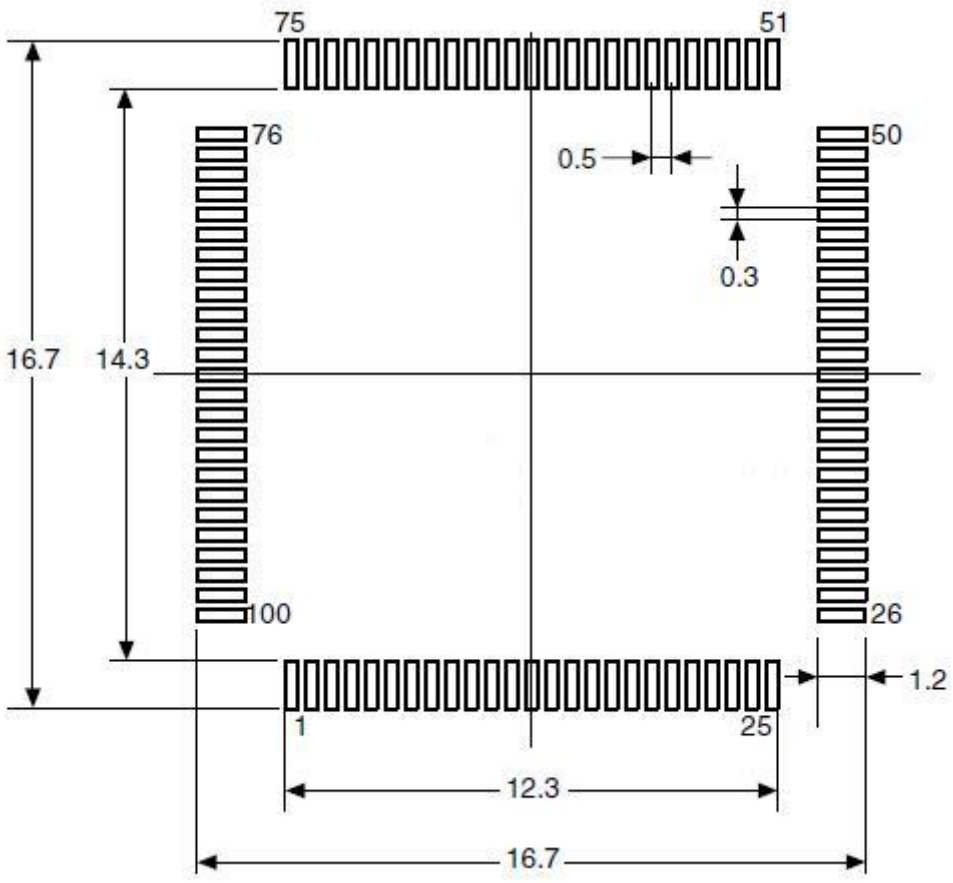
（1） All pins should be soldered to the PCB

Table45 LQFP100 Package Data

DIMENSION LIST（FOOTPRINT: 2.00）			
S/N	**SYM**	**DIMENSIONS**	**REMARKS**
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	16.000±0.200	LEAD TIP TO TIP
4	D1	14.000±0.100	PKG LENGTH
5	E	16.000±0.200	LEAD TIP TO TIP
6	E1	14.000±0.100	PKG WDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H（REF）	（12.00）	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

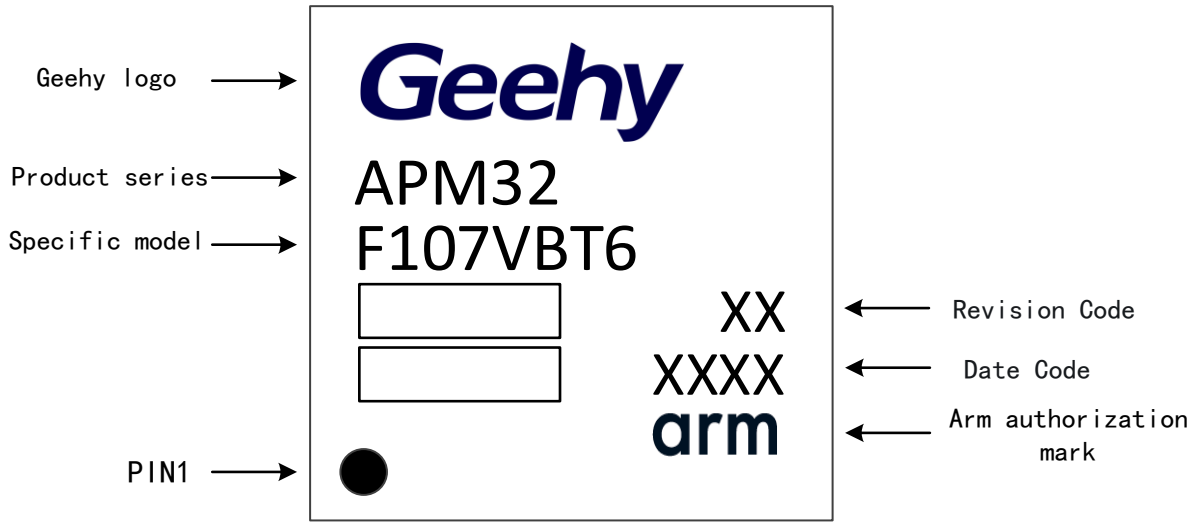
（1） Dimensions are displayed in mm

Figure 15 LQFP100-100 pins, 14×14mm recommended welding Layout



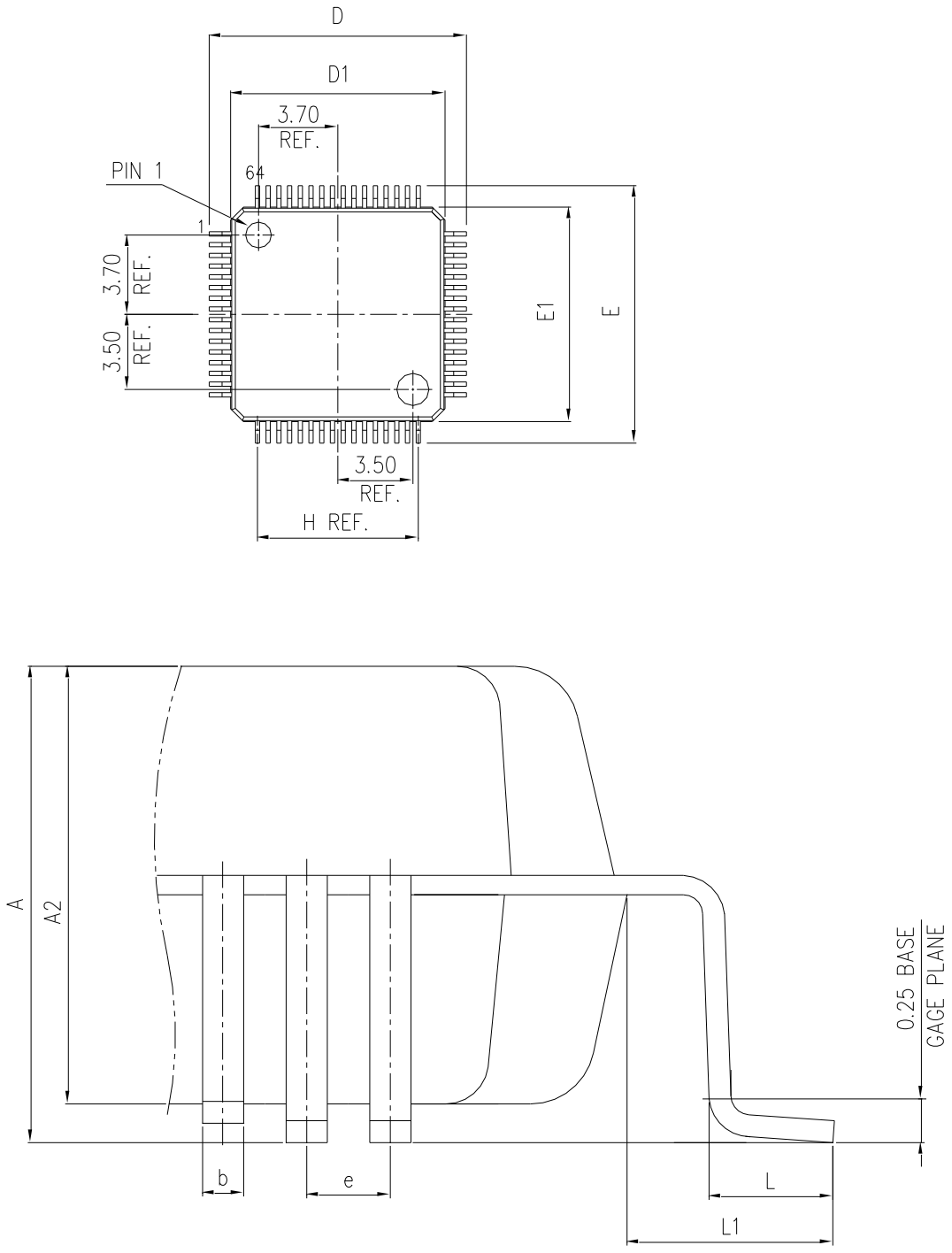
（1） Dimensions are expressed in mm

Figure 16LQFP100-100 pins, 14×14mm package identification



6.2. LQFP64 package diagram

Figure 17 LQFP64 Package Diagram



（1） The figure is not drawn to scale.

（2） All pins should be soldered to the PCB

Table46 LQFP64 Package Data

DIMENSION LIST（FOOTPRINT: 2.00）			
S/N	**SYM**	**DIMENSIONS**	**REMARKS**
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	12.000±0.200	LEAD TIP TO TIP
4	D1	10.000±0.100	PKG LENGTH
5	E	12.000±0.200	LEAD TIP TO TIP
6	E1	10.000±0.100	PKG WDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H（REF）	（7.500）	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

（1） Dimensions are expressed in mm

Figure 18 LQFP64-64 pins, 10×10mm recommended welding Layout

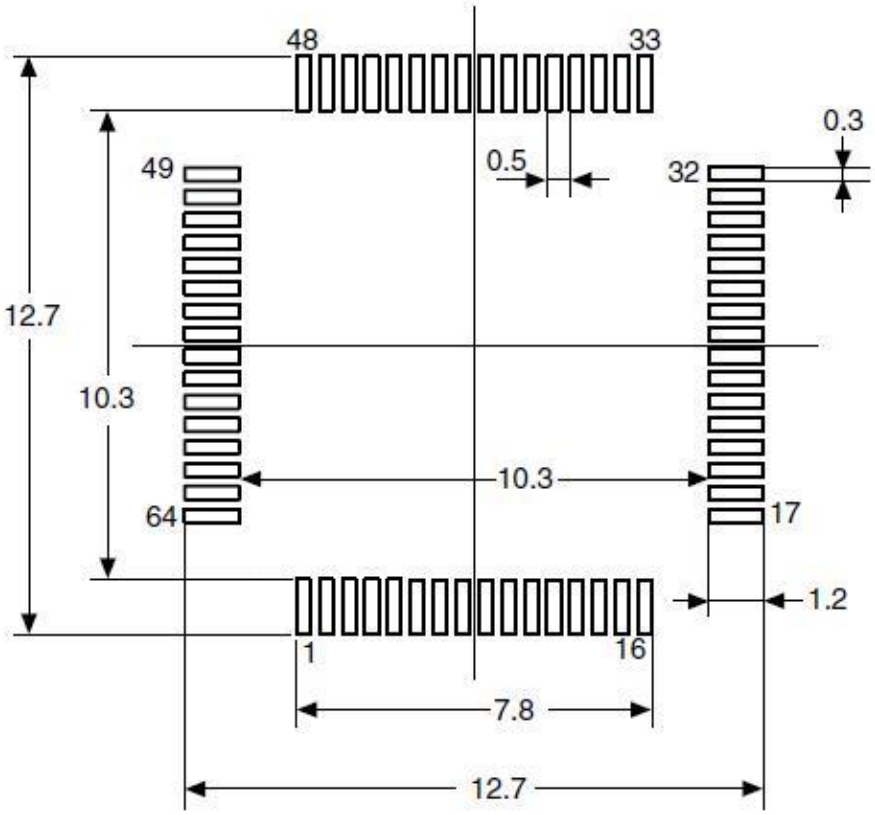
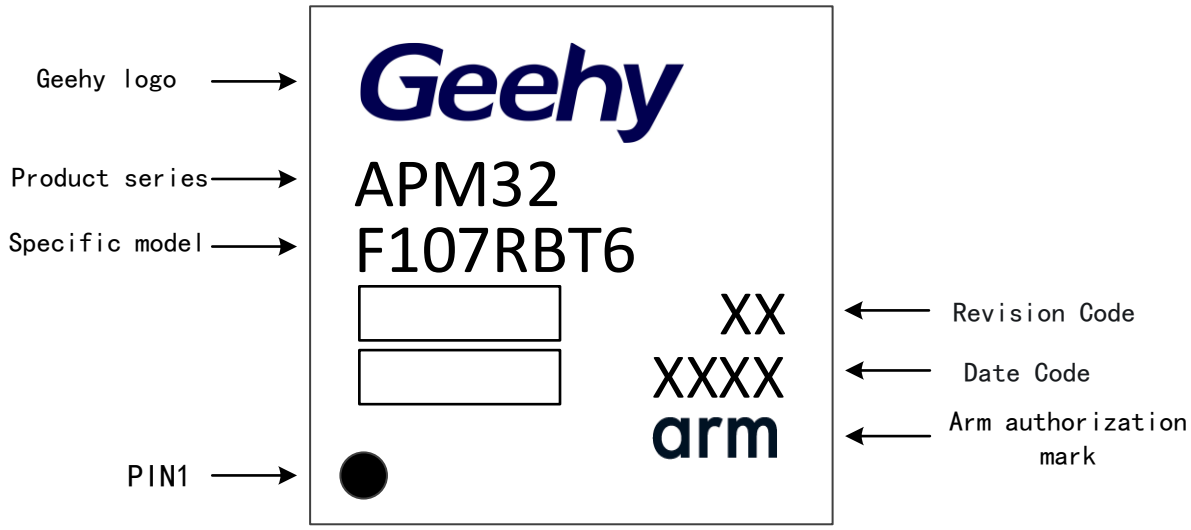


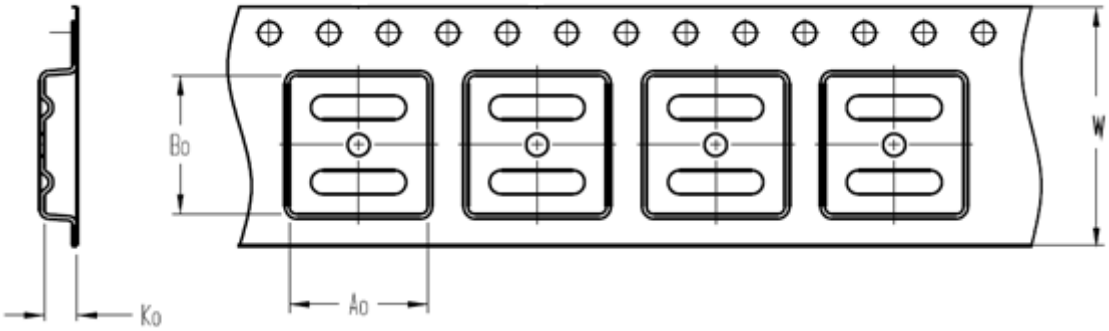
Figure 19 LQFP64-64 pins, 10×10mm package identification



7. Packaging information

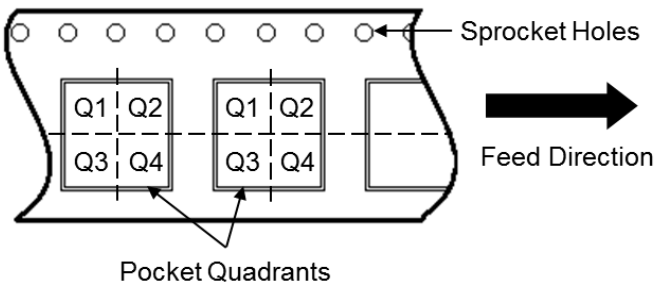
7.1. Reel packaging

Figure 20 Specification Drawing of Reel Packaging

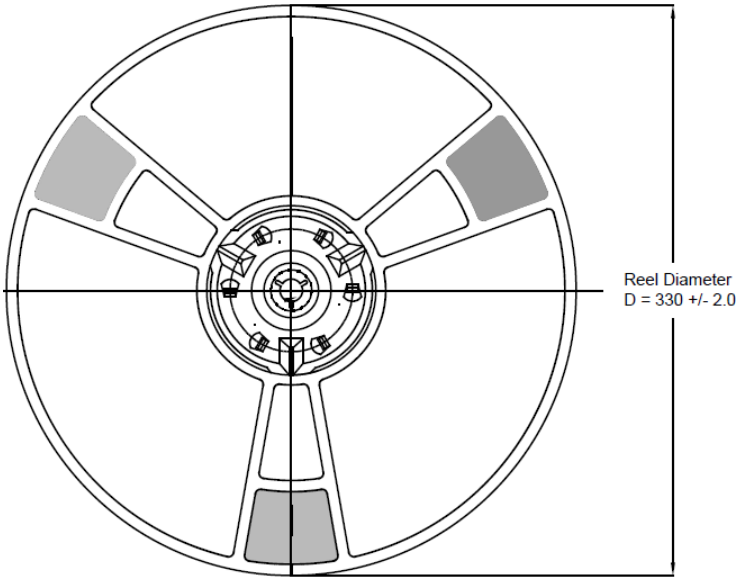


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



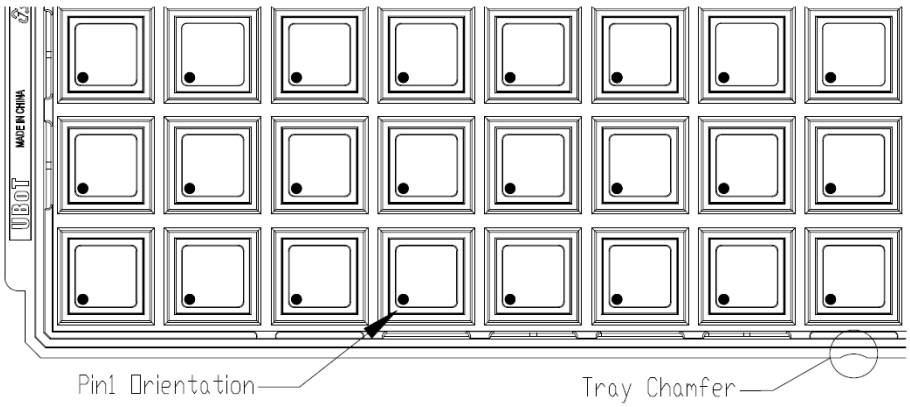
All photos are for reference only, and the appearance is subject to the product.

Table47 Reel Packaging Parameter Specification Table

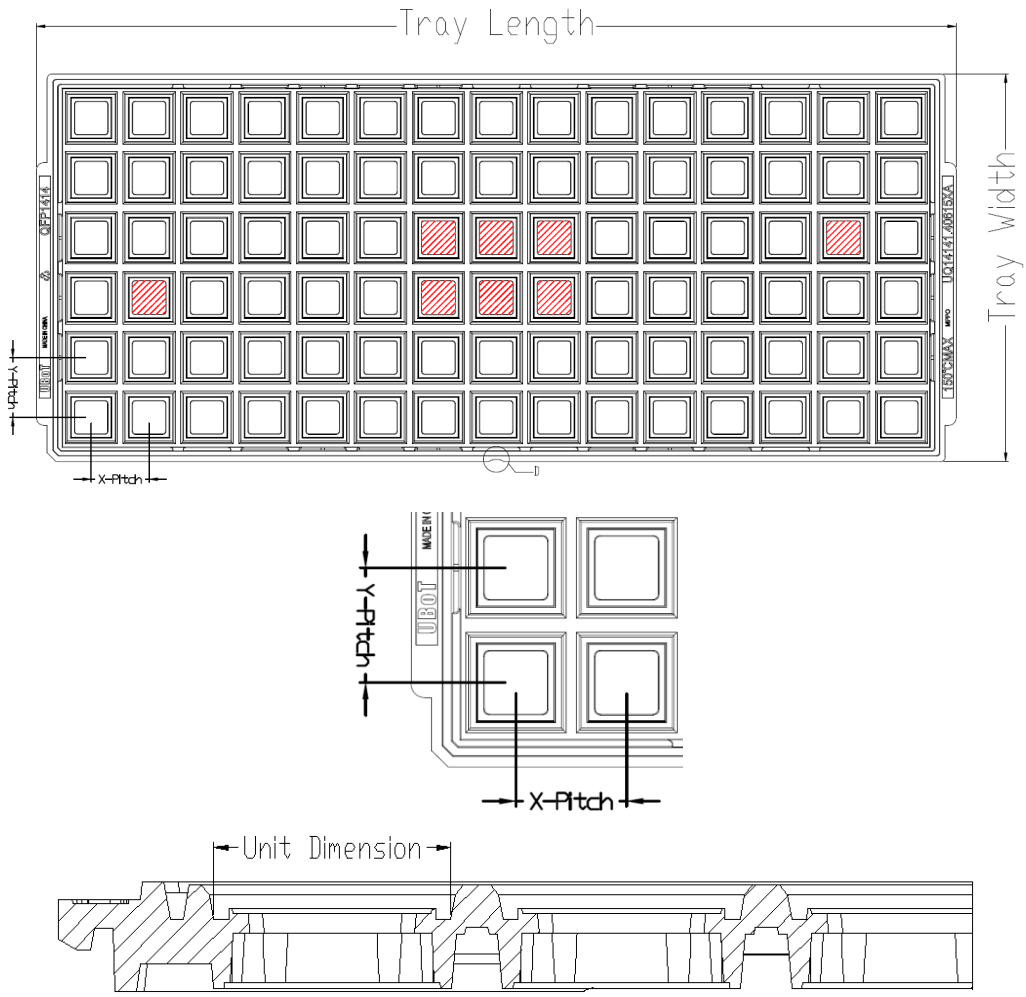
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
APM32F105R8T6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F105RBT6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F105RCT6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F107RBT6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F107RCT6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1

7.2. Tray packaging

Figure 21 Tray Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product.

Table48 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension（mm）	Y-Dimension（mm）	X-Pitch（mm）	Y-Pitch（mm）	Tray Length（mm）	Tray Width（mm）
APM32F105V8T6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F105VBT6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F105VCT6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F107VBT6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F107VCT6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F105R8T6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F105RBT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F105RCT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F107RBT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F107RCT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9

8. Ordering information

Figure 22 Product Naming Rules

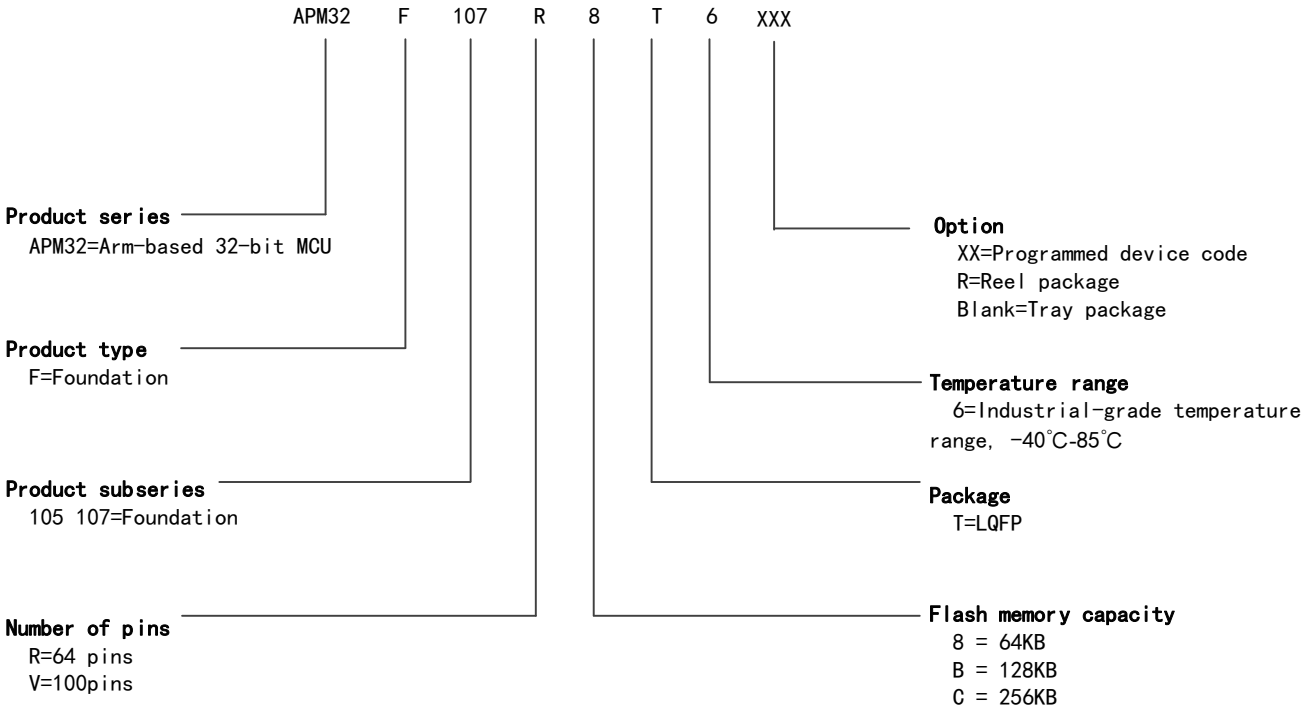


Table49 Ordering Information Table

Order Code	Flash（KB）	SRAM（KB）	Package	SPQ	Temperature Range
APM32F105V8T6	64	64	LQFP100	900	Industrial level -40℃~85℃
APM32F105VBT6	128	64	LQFP100	900	Industrial level -40℃~85℃
APM32F105VCT6	256	64	LQFP100	900	Industrial level -40℃~85℃
APM32F107VBT6	128	64	LQFP100	900	Industrial level -40℃~85℃
APM32F107VCT6	256	64	LQFP100	900	Industrial level -40℃~85℃
APM32F105R8T6	64	64	LQFP64	1600	Industrial level -40℃~85℃
APM32F105RBT6	128	64	LQFP64	1600	Industrial level -40℃~85℃
APM32F105RCT6	256	64	LQFP64	1600	Industrial level -40℃~85℃
APM32F107RBT6	128	64	LQFP64	1600	Industrial level -40℃~85℃
APM32F107RCT6	256	64	LQFP64	1600	Industrial level -40℃~85℃
APM32F105R8T6-R	64	64	LQFP64	1000	Industrial level -40℃~85℃
APM32F105RBT6-R	128	64	LQFP64	1000	Industrial level -40℃~85℃
APM32F105RCT6-R	256	64	LQFP64	1000	Industrial level -40℃~85℃
APM32F107RBT6-R	128	64	LQFP64	1000	Industrial level -40℃~85℃
APM32F107RCT6-R	256	64	LQFP64	1000	Industrial level -40℃~85℃

9. Commonly used function module denomination

Table50 Commonly Used Function Module Denomination

Chinese description	Short name
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External interrupt	EINT
Genera-purpose IO	GPIO
Multiplexing IO	AFIO
Wake up controller	WUPT
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
External memory controller	EMMC
Controller local area network	CAN
I2C interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC

10. Version history

Table51 Document Version History

Date	Version	Change History
September, 2023	1.0	New
October, 2024	1.1	Add flash storage time and erase cycle
June,2025	1.2	(1) Add attention points under general operating conditions (2) Add power-on/power-off characteristics

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